Toshiba

TC8512 Gouraud Shading Processor

Data Sheet

Features

- Gouraud shading at 8 Mpixels/second
- Bresenham line drawing
- Hidden surface removal (Z-buffer algorithm)
- Linear speed increase with parallel chips (up to 24 Mpixels/second) in Gouraud shading
- 16 MHz clock
- 200 mA maximum power consumption
- 144-pin flat pack, PGA

Description

The Toshiba TC8512 Gouraud Shading Processor (Figure 1) performs fast rendering of 3-dimensional solid objects and 2-dimensional lines and polygons.

Performance as high as 6 Mpixels/sec is achieved through hardware implementation of the Gouraud shading algorithm and Bresenham line drawing algorithm. Higher performance can be obtained by running two or four chips in parallel.

The TC8512 has four 16-bit ports. One port is the host interface through which commands and data, such as color intensity values and 3-D coordinates, are downloaded. The remaining three ports connect to video RAM (VRAM).

A VRAM is a type of DRAM which has two ports. One port is a random-access port similar to a standard DRAM interface. The other port is a serial-access port, through which data is clocked in sequence by loading it into an on-chip shift register.

The TC8512 gets maximum bandwidth from video RAM by using the serial and random-access ports simultaneously. Both the color intensity (I) and depth (Z) buffers are kept in VRAM. The I-buffer can directly feed the video DACs, or it can drive the address inputs of a color lookup table. The Z-buffer is used for hidden-surface removal while an image is drawn.

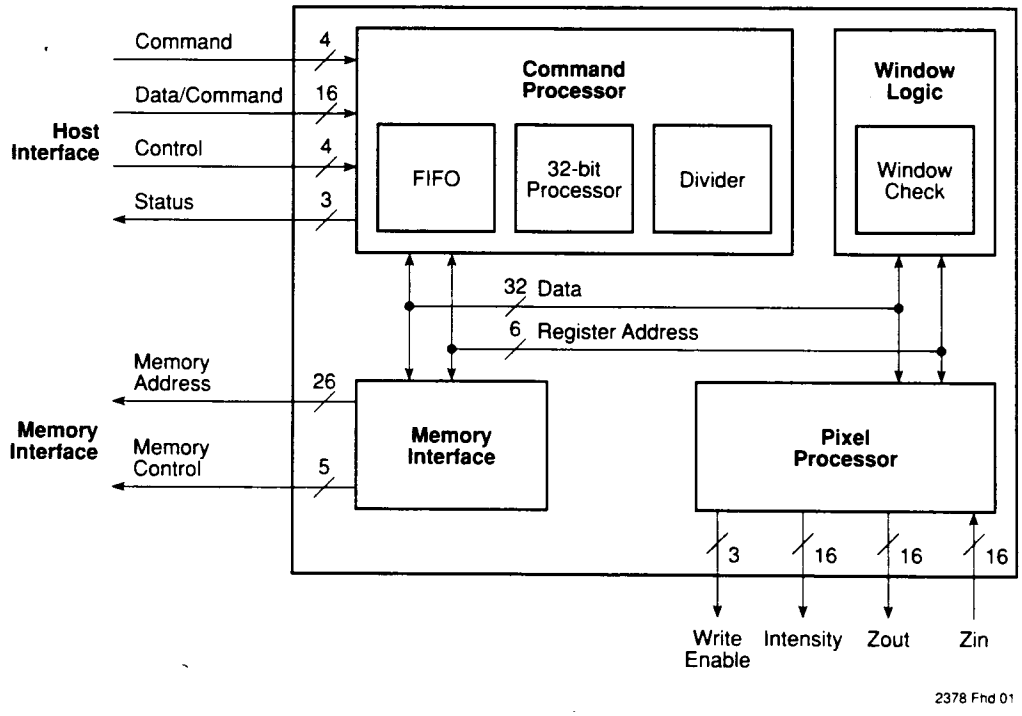

Figure 1. Internal Diagram

Gouraud Shading

Smooth shading of curved surfaces is performed using Gouraud shading, a technique in which I-values are calculated by linear interpolation between the I-values at the vertices of the polygon being drawn. This standard shading algorithm is described in textbooks on computer graphics, such as *Principles of Interactive Graphics* by William Newman and Robert Sproull (McGraw-Hill).

The TC8512 has separate digital differential analyzers (DDAs) for interpolating the I- and Z-values along the edges of polygons, and for interpolating between edges along a scan line.

In the TC8512 implementation, the polygons are triangles. The execution of a typical drawing command consists of several cycles of data downloaded from the host for each triangle, followed by many cycles to load the triangle into VRAM (Figure 2).

Constant Shading

The TC8512 also supports constant shading, in which all of the pixels within a triangle or trapezoid are assigned the same I- and Z-values. This can be used for fast rendering of 2-dimensional images and for initializing the I- and Z-buffers to a background value. With wide I- and Z-buffers and a small amount of external circuitry, constant shading may be performed at speeds up to 96 Mpixels/sec.

Line Drawing

The TC8512 also provides line drawing at speeds up to 6 Mpixels/sec. A Bresenham algorithm is used, which gives lines drawn at different angles the appearance of equal width. Depth cueing is performed by interpolating I and Z between the two endpoints of the line.

Z-Buffer Algorithm

The TC8512 uses a Z-buffer algorithm for hidden-surface removal. This algorithm assigns a Z-coordinate for every pixel on the screen. This value represents the distance from the observer to the closest surface at that point, and it is used to control write operations when adding features to an image.

For example, the image of two intersecting triangles shown below is rendered by first loading every pixel for the first triangle. Both the I- and Z-buffers are loaded. When the second triangle is drawn, the existing Z-coordinates are checked against the new values generated for the second triangle. For those pixels in which the depth is less (i.e., those parts of the triangle which are closer to the observer), the new I- and Z-values are loaded into VRAM. Where the depth is greater, the existing contents of VRAM remain unchanged (Figure 3).

To allow filling at the rate of one pixel for each VRAM cycle, the TC8512 has three ports: one to load the new

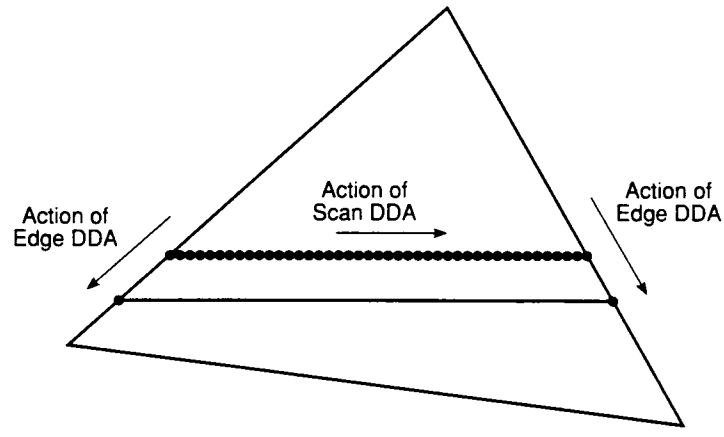

Figure 2. Gouraud Shading Diagram (showing interpolation)

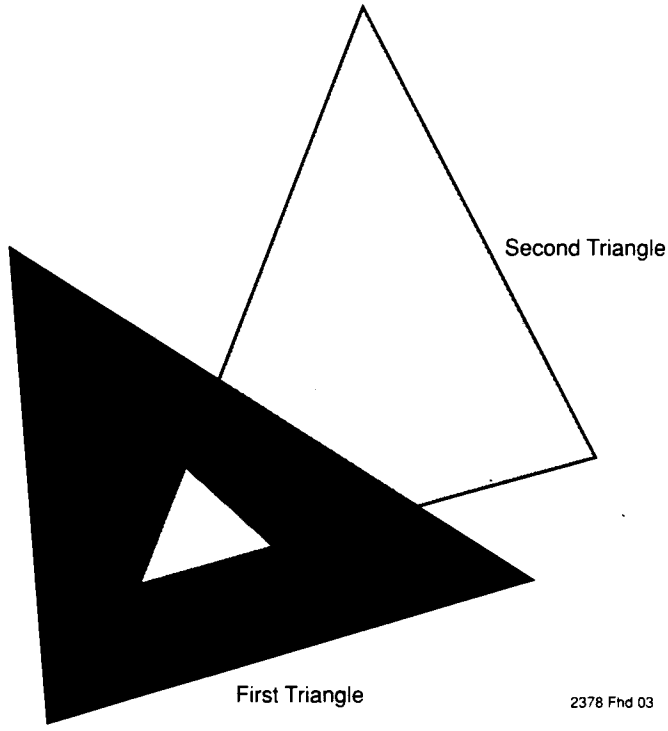

Figure 3. Intersecting Triangles

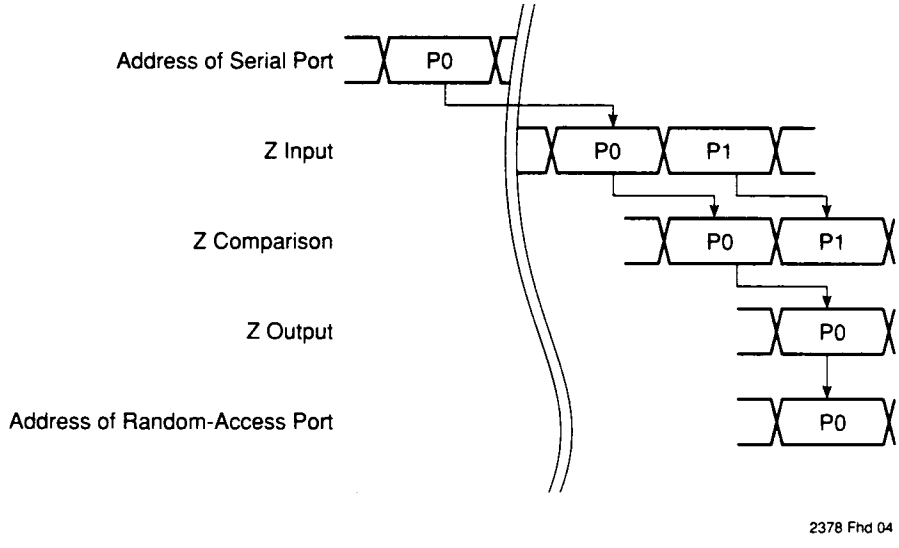

Figure 4. Pipelined Timing

I-value, one to load the new Z-coordinate, and one to read the existing Z-coordinate. The latter is connected to the serial port of the Z-buffer VRAMs, and it reads two cycles behind the random-access port to allow pipelining the comparison of the old and new Z-coordinates as shown in the following timing diagram (Figure 4).

Higher pixel rates are achieved in systems with parallel chips. For example, a system with two chips could use one for the odd pixels and the other for the even pixels, and these pixels would be generated simultaneously.

Clipping Window

The TC8512 can be programmed to inhibit drawing outside of a rectangular window defined in the screen coordinate system (Figure 5).

Raster Copy and Scaling

Two chips can be used as address generators in a configuration which allows rapid pixel block transfers from one memory to another. Magnification and reduction over a range from 1/64 to 64X are available in systems which implement this configuration (Figure 6).

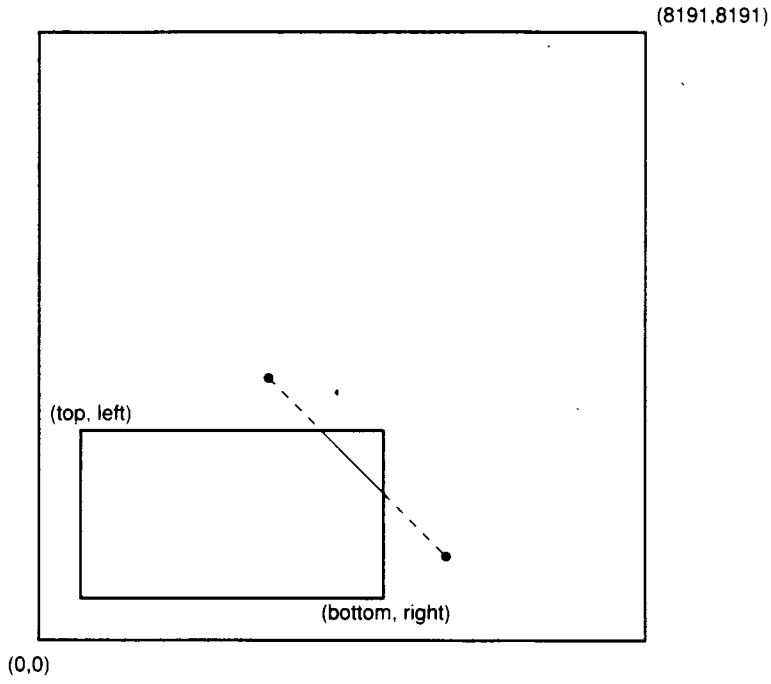

Figure 5. Clipping Window

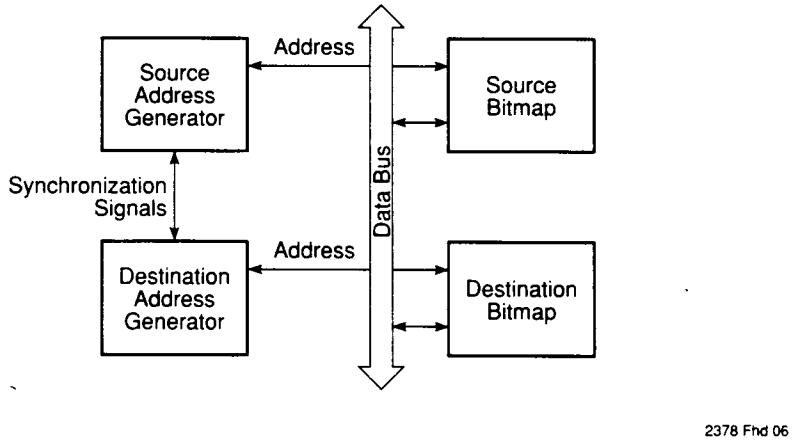

Figure 6. Address Generator Configuration

System Architecture

The TC8512 has two interfaces, one 16-bit port connected to the host processor and three 16-bit ports connected to VRAM. The VRAM ports share a common 26-bit address bus. A block diagram of a typical two-chip configuration is shown below (Figure 7).

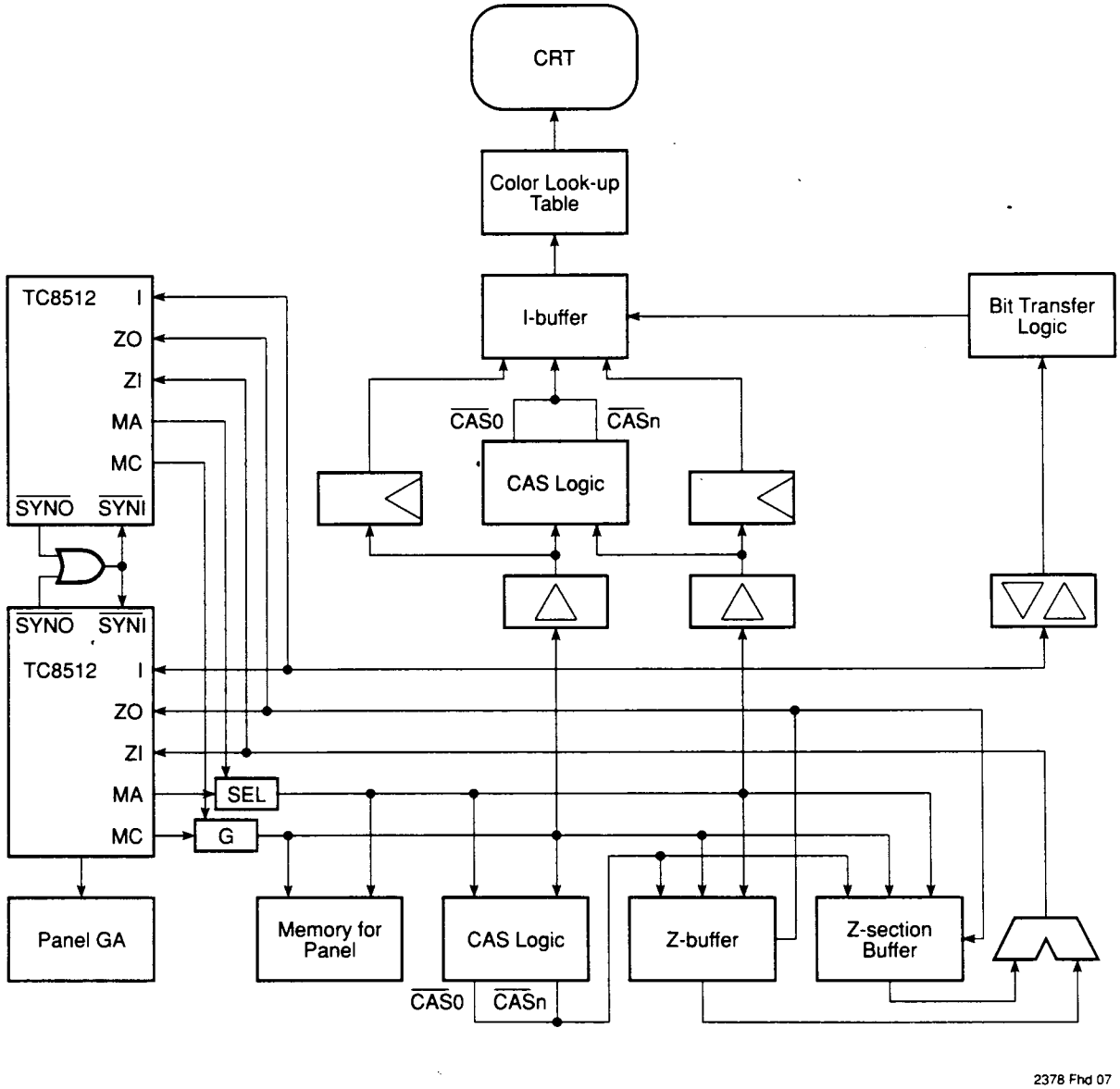

Figure 7. A Typical Two-Chip System

Host Processor Interface

The host processor interface receives commands and data, which are queued in an on-chip 20-bit x 16-level FIFO. It is intended that the host processor poll the NFLL line before downloading a new command. (It is also possible to use the NFLL signal to gate the DMA request when single-cycle DMA is used.)

The control signals consist of separate read and write strobe lines. Both of these signals are internally synchronized, which simplifies interface to asynchronous buses and buses running at frequency different from the TC8512.

Commands are transmitted on four signals intended for connection to the bus address. Each command also has data or subcommands which are sent on the data bus. To invoke a command, software writes data to one of the sixteen addresses decoded for the TC8512.

There are no byte enable signals; the TC8512 must be accessed strictly as a 16-bit device. Each pulse on the write strobe loads a new command, so any design which uses an 8-bit bus must perform the byte/word conversion externally.

VRAM Interface

The TC8512 generates a complete set of signals for interfacing to the serial and parallel ports of VRAM. Most signals simply require buffering for connection to the VRAM banks. The VRAM address, however, requires external multiplexing. The CAS signal also requires external logic.

In most systems, the host processor is required to provide refresh cycles. To allow the host to take control of the VRAM bus, a handshake has been provided using the WAIT and OEACK signals.

Two image transfer modes are available for uploading or downloading images between the host processor and VRAM. In one mode, each transfer moves a single 16-bit pixel. In the FAST mode, on the other hand, each transfer moves 16 one-bit pixels. The IMODE subcommand sets the image transfer mode. (See the Programming section, below.) The table below shows the relationship between the image transfer modes and various graphics functions.

HSP Functions	Memory Access Mode	
	1 pixel (16-bit)	16 pixels (1 bit each)
Gouraud up shading	●	
Constant shading		●
Depth Cuing	●	
Line Drawing color pixel pattern	●	●
Address Generation		●
Scaling Magnification/Reduction	●	
Image Data Out color pixel pattern	●	●
Image Data In pixel horizontal	●	●

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In the 1-pixel mode, the memory write logic controls the WE (write enable) signal. In FAST mode, the TC8512 generates a 16-bit mask pattern at the falling edge of the RAS signal (Figure 8). The external control circuit must latch the mask pattern, and use it to control the write-enable bit.

CAS for the VRAMs must be generated in external logic. At a minimum, the CAS signal from the TC8512 must be delayed by one clock period before being

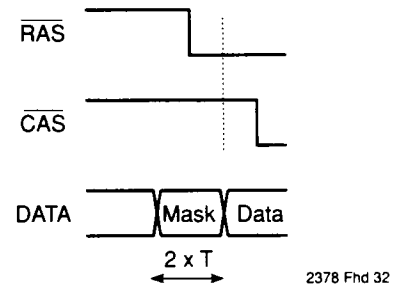

Figure 8. Mask Timing (Fast Mode)

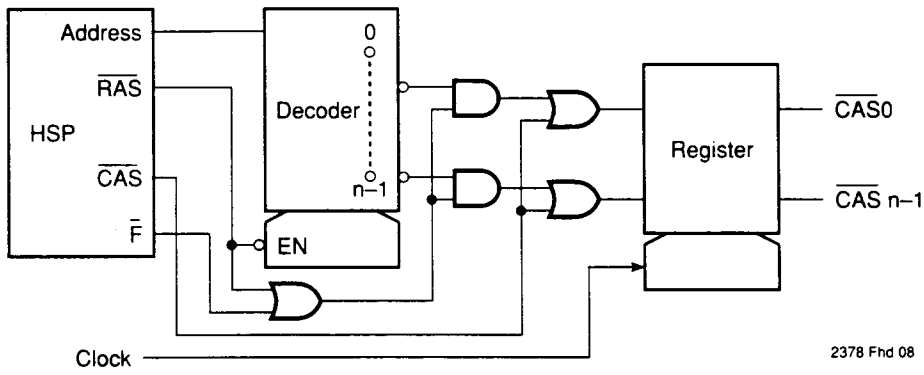

Figure 9. External CAS Generation

applied to VRAM. If FAST mode (i.e., 16-pixel mode) is not selected using the IMODE subcommand or if both FAST mode and FS mode (i.e., reduced CAS timing, as selected by the HCONTROL subcommand) are selected, an external circuit must be provided to decode the low address bits (Figure 9). In this case, the CAS signal from the TC8512 is used to enable the CAS signals applied to VRAM.

Address Generator Configuration

In the two-chip address generator configuration, the $\overline{SYNI}$, $\overline{SYNO}$, $\overline{PXEND}$, and $\overline{PYEND}$ synchronization signals are connected as shown below. The $\overline{SYNI}$ and $\overline{SYNO}$ signals are connected differently in other configurations, and the $\overline{PXEND}$ and $\overline{PYEND}$ signals are not used at all (Figure 9).

Multiprocessor Configurations

There are two ways to use multiple chips to achieve higher performance. In one method, each chip has its own I- and Z-buffers, and the pixels in these buffers are interleaved. For example, in a two-chip system (Figure 10), one chip handles the even pixels while the other chip handles the odd pixels. In a four-chip system, each chip handles every fourth pixel, and the chips are staggered one pixel apart.

The other method is specific to RGB color systems. Here, separate I-values are used to drive the red, green, and blue video DACs. In this configuration, one chip handles interpolation in Z and one of the I-values, while the other chip handles the other two I-values.

The former method provides faster drawing rates than a single processor, while keeping the same number of I-bits. The latter method provides the same drawing rate as a single processor, while increasing the number of I-bits. The latter method is used where the I-bits are interpreted directly as the color, rather than as an index into a color lookup table. (Lookup tables might be used with the latter method, but their purpose would be to correct for non-linearities in the conversion of digital I-values into the colors perceived by the eye.)

In any multi-chip configuration, it is necessary to synchronize the WAIT input signal (which is used during the VRAM refresh cycle) to prevent skewing. Shown below (Figure 11) is an example in which an external flip-flop is used to distribute the WAIT signal. The trailing edge of the TC8512 clock is input as the flip-flop clock.

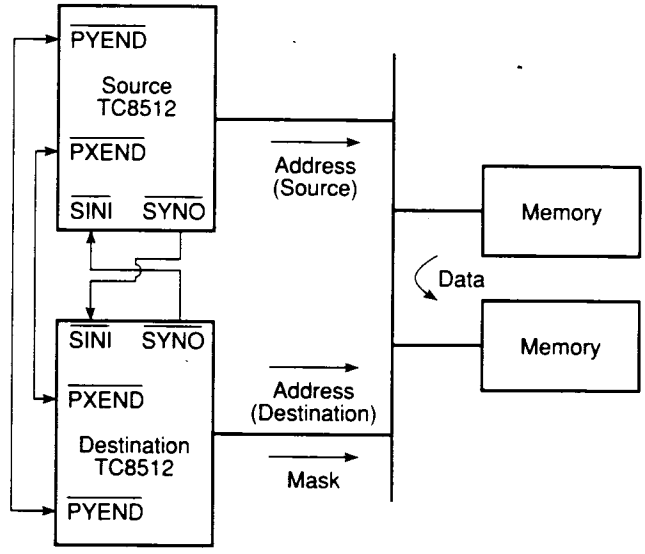

Figure 10. Two-Chip System

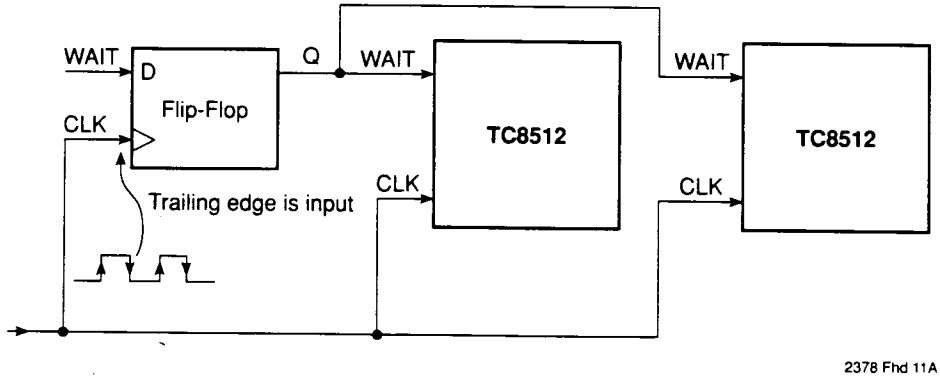

Figure 11. Synchronization of WAIT Signal

Interleaved Pixels

When multiple chips are used to handle interleaved pixels, the $\overline{SYNO}$ outputs are ORed together and used to drive the $\overline{SYNI}$ inputs, as shown below (Figure 12) for a four-chip system. A similar configuration is used for a two-chip system.

The INIT command and HCONTROL subcommand are used to enable the two- or four-chip configurations (i.e., CSCD = 1 or 2, EXSYN = 1). The commands which set I-, Z-, X- and Y-values are downloaded to all chips simultaneously.

RGB Color

When two chips are used to drive an RGB color system (Figure 13), one chip handles the Z-buffer algorithm and one of the colors (red, green, and blue). The second chip handles the other two colors, using its Z logic to interpolate one of the colors. The $\overline{SYNI}$ and $\overline{SYNO}$ signals are handled in the same manner used for interleaved pixels.

Unlike the interleaved pixels configuration, the INIT command initializes the chips for the uniprocessor configuration (i.e., CSCD = 0). The ZCONTROL subcommand enables hidden surface removal (i.e., ZCK = 1). The HCONTROL subcommand selects output of the internally calculated Z-coordinate (ZI = 0) and external sync (EXTSYN = 1). The commands which download X- and Y-coordinates are downloaded to both chips simultaneously, however the Z-values and each color's I-values are specific to each chip.

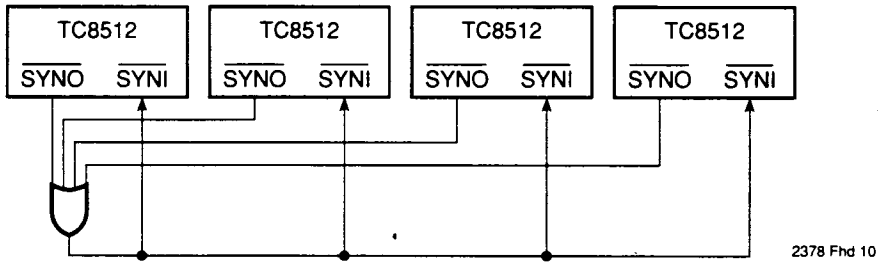

Figure 12. Four-Chip System

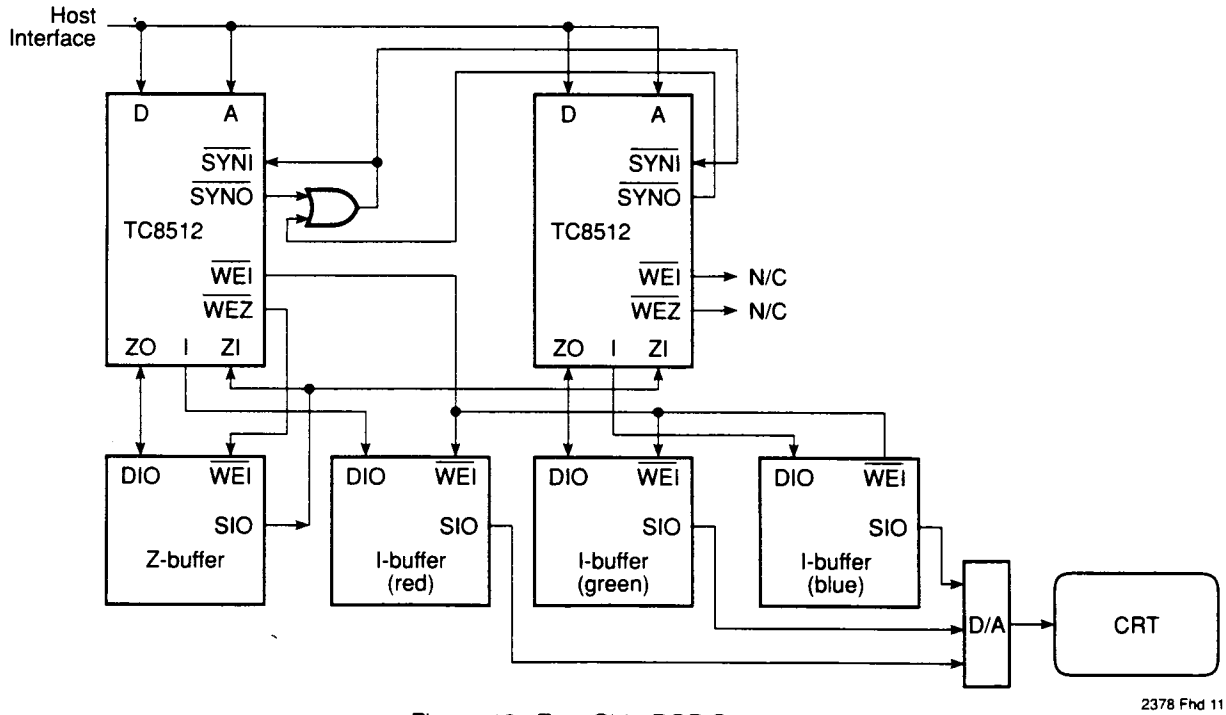

Figure 13. Two-Chip RGB System

Programming

This section describes the operation of the TC8512 as seen by the programmer, including the coordinate system, default mode settings, and commands.

Screen Coordinate System

The origin of the coordinate system is the bottom left corner of the screen, at the closest distance to the observer. The X-coordinate increases toward the right, the Y-coordinate increases toward the top, and the Z-coordinate increases with greater distance from the observer. The X- and Y-coordinates are unsigned binary numbers up to 13 bits in length. The Z-coordinate is an unsigned binary number up to 16 bits in length. A screen resolution of up to 8192 x 8192 pixels can be accommodated.

Default Modes

When the TC8512 is given an INIT command, internal mode settings get set to the following default values:

- Polygon drawing mode is Gouraud shading. (See PMODE subcommand.)
- Line drawing mode does not overwrite background pixels. (See LMODE subcommand.)
- When an image is uploaded or downloaded between the host and VRAM, 16-bit pixels are assumed. (See IMODE subcommand.)
- Hidden-surface removal and depth sectioning are both disabled. (See ZCONTROL subcommand.)
- Hardware control modes are all 0. (See HCONTROL subcommand.)
- Transparency pattern has all bits set (i.e., no pixels are masked). (See TPATTERN subcommand.)
- Clipping window boundaries are at their maximum range (0 and 8192, in both X and Y). (See WINDOW subcommand.)
- Constant Z-sectioning depth is at its maximum value (FFFFh). (See SECTION subcommand.)
- Foreground and background colors for 2-dimensional line drawing are 1 and 0, respectively. (See COLOR subcommand.)
- Cyclic line pattern produces a solid line. (See LPATTERN subcommand.)
- A bit-planes are enabled for writes. (See MASK subcommand.)
- Magnification/reduction scale (only used with the two-chip address generator configuration) is 1 to 1. (See SCALE subcommand.)
- Line status is waiting for the first endpoint of a line or polyline. (See LSTATUS command.)

Commands

In the command descriptions that follow the summary table, on the next page, the four bits which invoke the command are shown to the left of the data applied to the sixteen-bit data bus. Typically, the command bits will come from the low address lines on the bus of the host processor, so that commands are invoked by writing data to specific bus addresses.

Command	Hex Code	Data	Description
INIT	F	Initialization	System configuration and default-mode setting.
AUX	E	Auxiliary commands	Specifies various subcommands. The AUX command is followed by one or more PARM commands.
PARM	D	Parameters	Data for the subcommands specified in the AUX, IMG, and ADDR commands.
(reserved)	C		
I	1	Color-index value (I-value)	Downloads a 16-bit I-value for the next line or polygon vertex.
Z	2	Z-coordinate (depth value)	Downloads a 16-bit Z-coordinate for the next line or polygon vertex.
Y	3	Y-coordinate	Downloads a 13-bit Y-coordinate for the next line or polygon vertex.
X	4	X-coordinate	Downloads a 13-bit X-coordinate for the next line or polygon vertex.
T1X	5	Triangle X-coordinate (LMODE 1)	In line-drawing mode 1, downloads a 13-bit X-coordinate for the first vertex of a triangle.
T2X	6	Triangle X-coordinate (LMODE 2)	In line-drawing mode 2, downloads a 13-bit X-coordinate for the first vertex of a triangle.
(reserved)	7		
LX	8	Line X-coordinate	Downloads a 13-bit X-coordinate for the first endpoint of a line or polyline.
IMG	9	Image coordinates	Used with PARM commands to specify a transfer-direction and a rectangular region of the I-buffer for subsequent transfer by the PTRN command.
PTRN	0	Pattern transfer	Transfers 16 bits of pixel data to or from the host. The direction of transfer is controlled by the IMG command.
ADDR	A	Address transfer	*(Used only in the two-chip address generator configuration.)* Used with PARM commands to transfer a rectangular region of memory between source and destination.
PX	B	Polyline X-coordinate	Downloads a 13-bit X-coordinate for the endpoints of a polyline, after the first endpoint has been downloaded with the LX command.

INIT Command

Command				Command															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	AM	CT	ADDR						CSCDO		CSCDNO		SIZE			

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First command given following reset initialization. It is also used whenever any of the modes it controls need to be changed. Note that all other modes get set to their default values.

AM — Selects the pixel cache organization. 0 selects 4 x 4; 1 selects 16 x 1.

CT — Enables the pixel cache. 0 is cache disabled; 1 is cache enabled. (The pixel cache increases the speed of some graphics operations. Early versions of the TC8512 do not implement the pixel cache. Be sure your version implements this feature before enabling this bit.)

ADDR — Sets the horizontal line length. This is used to generate linear addressing for VRAM. The ADDR field is a six-bit code, which is encoded as shown below:

Code	Line Length (in pixels)
000000	256
000001	320
000010	384
000011	448
000100	512
000101	576
000110	640
000111	704
010010	768
010011	832
001000	1024
001001	1088
001010	1152
001011	1216
010110	1280
010111	1344
100010	1536
100011	1600
001100	2048
001101	2112
001110	2176
001111	2240
011010	2304
011011	2368
100110	2560
100111	2624
011100	4096
011101	4160
011110	4352

011111	4416
101010	4608
101011	4672
101100	8192
101101	8256
101110	8704
101111	8768

CSCDO Specifies the number of chips in a multichip configuration. 0 is one chip; 1 is two chips; 2 is four chips.

CSCDNO Specifies the unit number in a multichip configuration. Legal values are 0, 1, 2, and 3.

SIZE Specifies the page size, so the TC8512 knows when to reload the row address into VRAM. The SIZE field is a four-bit code, which is encoded as shown below:

Code	Page Size (in bytes)
0000	256
0001	512
0010	1K
0011	2K
0100	4K
0101	8K
0110	16K
0111	32K

AUX and PARM Commands

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	Subcommand															
1	1	0	1	Data															

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The AUX and PARM commands are used together to execute several subcommands. The AUX command is issued first, with the Subcommand in its data field. Then one or more PARM commands is issued, with the data relevent to the subcommand in its data field.

PMODE Subcommand

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	Shading Mode															

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Selects one of two polygon shading modes. 0 selects Gouraud shading; 1 selects constant shading. All other values of the shading mode are reserved for future expansion.

LMODE Subcommand

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	0	1	Line Drawing Mode															

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Selects one of three line drawing modes. Two of these modes are intended for 2-dimensional line drawing, in which a cyclic pattern can be used to create dotted and dashed lines. (For more information, see the description of the LPATTERN subcommand.) In mode 0, pixels in the dots or dashes are loaded from a register which specifies the foreground I-value. The parts of the line between the dots or dashes are loaded from another register, which specifies the background I-value.

In mode 1, only the foreground pixels are loaded. The background pixels are left undisturbed. This provides a transparent background, in which empty spaces between dots or dashes do not overwrite the existing contents of the I-buffer.

In mode 2 (3-D line drawing), the cyclic pattern is ignored. The I-values are interpolated between the line endpoints, which provides depth cueing. If hidden-surface removal is enabled (using the ZCONTROL subcommand), the Z-coordinates are also interpolated between endpoints.

All other values of the line drawing mode are reserved for future expansion.

IMODE Subcommand

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	0	1	Image Data Transfer Mode															

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Selects the image transfer mode, for uploading or downloading images between the host processor and VRAM. 0 selects 16-bit pixels, one per transfer; 1 selects 1-bit pixels, 16 per transfer. The latter mode requires external logic to steer the pixels onto the I-bus (the mode setting only affects the VRAM addressing).

All other values of the image data transfer mode are reserved for future expansion. In the two-chip address generator configuration, the 16-bit pixel mode must be used (the default mode).

The image transfer mode remains fixed until the next INIT command or IMODE subcommand is executed.

ZCONTROL Subcommand

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	1	0	0	0	0	0	0	0	0	0	ZCK	ZSC	ZSW	0	0	0	0

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Controls hidden-surface removal and two forms of Z-sectioning.

ZSW — Selects the source of Z-sectioning data. 0 selects a constant sectioning depth loaded using the SECTION subcommand; 1 selects a variable sectioning depth from an external Z-sectioning buffer.

ZSC — Controls depth sectioning. 0 disables it; 1 enables it. (Early versions of the TC8512 do not implement depth sectioning. Be sure your version implements this feature before enabling this bit.)

ZCK — Controls hidden-surface removal. 0 disables it; 1 enables it.

HCONTROL Subcommand

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	0	1	0	0	CORR	0	EXSYN	RMW	0	FS	BMSK	0	0	0	ZI	IE	ZE	ZSCE

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Defines miscellaneous hardware control modes.

CORR — Controls subpixel correction. 0 disables it (I- and Z-values are rounded); 1 enables it.

EXSYN — Enables the $\overline{\text{SYNI}}$ input. 0 is for single-chip configurations; 1 is for multichip configurations. EXSYN is also used for image-data input synchronization.

RMW — Enables read/modify/write cycles to VRAM. 0 is for separate read and write cycles; 1 is for read/modify/write cycles.

FS — Enables shorter CAS-only cycles (only used when constant shading and page mode access are selected). 0 is longer cycles (4 clock periods); 1 is shorter cycles (2 clock periods).

BMSK — Enables the write pulse when bit mask data is being presented (only used in 16-pixel mode). 0 is write pulse inhibited; 1 is write pulse enabled.

ZI — Selects the buffer being accessed when data is being uploaded or downloaded between the host processor and VRAM. During download, 0 sends Z-data out the Z-output bus; 1 sends I-data out the Z-output bus. During upload, 0 reads from the I-buffer; 1 reads from the Z-buffer.

IE — Enables the write pulse on the I-bus when an I-value is being presented. 0 is write pulse inhibited; 1 is write pulse enabled.

ZE — Enables the write pulse on the Z-bus when a Z-coordinate is being presented. 0 is write pulse inhibited; 1 is write pulse enabled.

ZSCE — Enables the write pulse on the Z-bus when Z-sectioning data is being presented (only used when Z-sectioning is enabled). 0 is write pulse inhibited; 1 is write pulse enabled.

TPATTERN Subcommand

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
1	1	0	1	Transparency Pattern															

2378 Drw 08

Specifies a transparency pattern. This is a mask which is ANDed with the write enable for each pixel, to allow existing images to be seen through new images loaded into VRAM. The mask is a 4 x 4 array of bits, addressed by the two LSBs of the X- and Y-addresses. If a mask bit is clear, pixels which match that bit's X and Y LSBs are not written to VRAM.

The correspondence between bits in the transparency pattern and bits in the mask is shown in the table below. Gouraud shading and 3-dimensional line drawing ignore the transparency mask.

The transparency pattern remains fixed until the next INIT command or TPATTERN subcommand is executed.

2 LSBs of Y \ 2 LSBs of X	00	01	10	11
00	0	1	2	3
01	4	5	6	7
10	8	9	10	11
11	12	13	14	15

2378 Fhd 12

WINDOW Subcommand

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
1	1	0	1	Top Left X-Coordinate															
1	1	0	1	Top Left Y-Coordinate															
1	1	0	1	Bottom Right X-Coordinate															
1	1	0	1	Bottom Right Y-Coordinate															
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

2378 Drw 09

Specifies a clipping window within the screen coordinate system. Drawing is inhibited outside of the clipping window. Pixels on the border of the clipping window are not clipped. The boundary values of the clipping window remain fixed until the next INIT command or WINDOW subcommand is executed.

SECTION Subcommand

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
1	1	0	1	Z-Sectioning Depth (Constant)															

2378 Drw 10

Define a Z-sectioning depth. This value is only used for constant Z-sectioning (see the description of the ZCONTROL subcommand). Transparency-pattern drawing is inhibited for pixels with a greater Z-coordinate (i.e., further from the observer).

COLOR Subcommand

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
1	1	0	1	Foreground Color															
1	1	0	1	Background Color															

2378 Drw 11

Define the foreground and background colors (I-values) used for line drawing. In 2-dimensional line drawing, a cyclic pattern can be used to create dotted and dashed lines. (For more information, see the description of the LPATTERN subcommand.) Pixels in the dots or dashes are loaded with the foreground color. The parts of the line between the dots or dashes can be loaded with the background color.

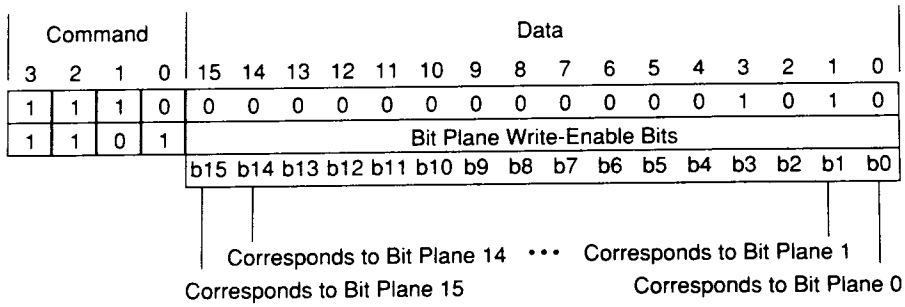
LPATTERN Subcommand

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
1	1	0	1	Line Pattern (bits 31-16)															
1	1	0	1	Line Pattern (bits 16-0)															

2378 Drw 12

Specifies a line pattern. This is a mask applied cyclically during 2-dimensional line drawing to create various dotted and dashed effects. These bits are ANDed with the write enable for each pixel. The first pixel is ANDed with bit 31 of the mask, the second pixel with bit 30, etc. For example, a solid line would have all bits set (11111111...1111) while a dotted line would have alternating set and clear bits, such as (11001100...1100).

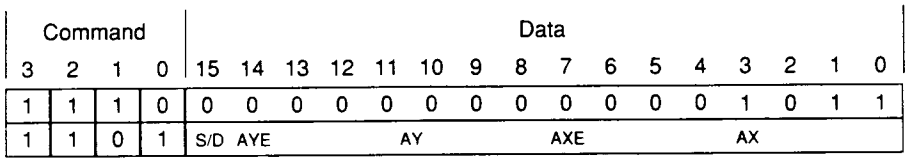
MASK Subcommand



2378 Drw 13

Specify a mask to inhibit writes to individual bit planes. This mask is initialized after switching to 16-pixel mode.

SCALE Subcommand



2378 Drw 14

Specify mode settings for the two-chip address generator configuration. The magnification or reduction scale factor is independent in each dimension. The scale factor is:

(source count +1) / (destination count + 1)

For example, a value of 9 in the source chip and a value of 0 in the destination chip would result in a magnification factor of 10X.

S/D	Select source or destination mode. 0 is destination; 1 is source.
AYE	For magnification in Y, this bit is 0 in the source chip and 1 in the destination chip. For reduction in Y, this bit is 1 in the source chip and 0 in the destination chip.
AY	Magnification or reduction count for Y-coordinate.
AXE	For magnification in X, this bit is 0 in the source chip and 1 in the destination chip. For reduction in X, this bit is 1 in the source chip and 0 in the destination chip.
AX	Magnification or reduction count for X-coordinate.

LSTATUS Subcommand

Command				Data														
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	INV	END	0	0	0	0

2378 Drw 15

Controls line drawing. There are two states: a state which controls termination of a line or polyline (i.e., chained vectors), and a state which controls visibility. An INIT command or the last endpoint of the previous line or polyline will leave the TC8512 waiting for the first endpoint of the next line or polyline. After downloading the first endpoint, an LSTATUS subcommand is issued to enable visibility. Intermediate endpoints may be downloaded without any intervening LSTATUS subcommands. Before the last endpoint is downloaded, an LSTATUS subcommand is used to identify the last endpoint as the termination of the polyline.

Between any two points in a polyline, the LSTATUS subcommand can be used to selectively inhibit drawing of individual line segments. A second LSTATUS subcommand is used to re-enable drawing, if desired.

INV — Enables line drawing between the previous endpoint and next endpoint. 0 enables drawing (i.e., visible); 1 inhibits drawing (i.e., invisible).

END — Specifies whether the next endpoint will terminate a line or polyline. 0 is no termination; 1 is termination.

I Command

Command				Data														
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	I-Value															

2378 Drw 16

Downloads an I-value for the next line or polygon vertex. This value is a 16-bit unsigned integer.

Z Command

Command				Data														
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	Z-Coordinate															

2378 Drw 17

Downloads a Z-coordinate for the next line or polygon vertex. This value is a 16-bit unsigned integer. The value increases with greater distance from the observer.

Y Command

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	Y-Coordinate															

2378 Drw 18

Downloads a Y-coordinate for the next line or polygon vertex. This value is a 13-bit unsigned integer. The value increases from the bottom to the top of the screen.

X Command

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	X-Coordinate															

2378 Drw 19

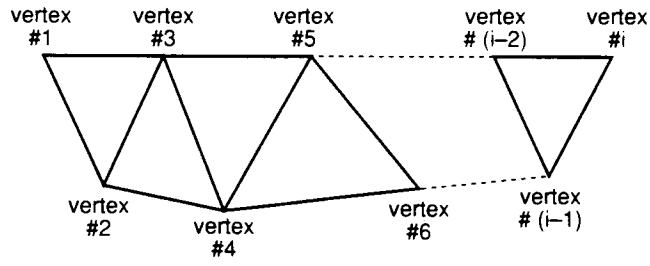
Downloads an X-value for the next line or polygon vertex. This value is a 13-bit unsigned integer. The value increases from the left to the right of the screen. The order of I, Y, and Z is arbitrary, but each endpoint or vertex must be terminated by an X-coordinate. The T1X, T2X, and LX commands are special forms of the X command used to indicate the beginning of a triangle or line.

T1X Command

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	X-Coordinate															

2378 Drw 20

In line-drawing (LMODE) mode 1, downloads an X-value for the first vertex of a triangle. This value is a 13-bit unsigned integer. The value increases from the left to the right of the screen. The order of I, Y, and Z is arbitrary, but the vertex must be terminated by an X-coordinate. Subsequent connected triangles may be drawn as shown below.



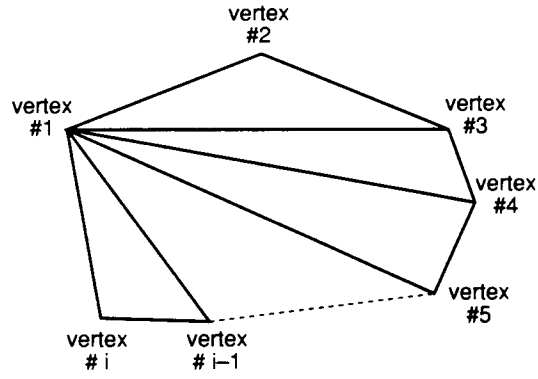
2378 Fhd 13

T2X Command

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	X-Coordinate															

2378 Drw 21

In line-drawing (LMODE) mode 2, downloads an X-coordinate for the first vertex of a triangle. This value is a 13-bit unsigned integer. The value increases from the left to the right of the screen. The order of I, Y, and Z is arbitrary, but the vertex must be terminated by an X-coordinate. Subsequent connected triangles may be drawn as shown below.



2378 Fhd 14

LX Command

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	X-Coordinate															

2378 Drw 22

Downloads an X-coordinate for the first endpoint of a line or polyline. This value is a 13-bit unsigned integer. The value increases from the left to the right of the screen. The order of I, Z, and Y is arbitrary, but the endpoint must be terminated by an X-coordinate.

IMG and PARM Commands

Command				Data														
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	TO	0	RW
1	1	0	1	X-Coordinate															
1	1	0	1	Y-Coordinate															
1	1	0	1	X-Coordinate															
1	1	0	1	Y-Coordinate															

2378 Drw 23

One IMG command and four PARM commands, used in sequence, specify a rectangular region of the I-buffer for transfer to or from the host processor. If the first coordinate pair specified in the PARM commands is above and to the left of the second coordinate pair, the orientation of the data remains the same. If not, the region will be flipped in one or both dimensions. For example, if the first coordinate pair has a smaller Y-coordinate than the second, the region will be flipped in the Y-dimension.

A 16-bit data transfer occurs when the PTRN command is used. The IMODE subcommand selects whether a transfer corresponds to one 16-bit pixel or 16 1-bit pixels.

TO — During a transfer from the host to the I-buffer in 16-pixel mode, specifies whether background pixels are overwritten with the background color or left undisturbed. 0 is overwritten (opaque); 1 is undisturbed (transparent).

RW — Specifies the direction of transfer. 0 is host to I-buffer; 1 is I-buffer to host.

PTRN Command

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	Pixel Data															

2378 Drw 24

Transfers 16 bits of data between the host and the I-buffer. The direction of transfer is controlled by the IMG command.

ADDR and PARM Commands

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	Address Generator Selection															
1	1	0	1	X-Coordinate															
1	1	0	1	Y-Coordinate															
1	1	0	1	X-Coordinate															
1	1	0	1	Y-Coordinate															

2378 Drw 25

These commands are used, *only in the two-chip address generator configuration,* to transfer a rectangular region of memory between source and destination.

A sequence of one ADDR command and four PARM commands is issued twice. The first sequence specifies a rectangular block of pixels in the source region of memory. The second sequence specifies a block in the destination region. After both sequences are issued, a transfer of pixels between source and destination occurs.

In each sequence, the ADDR command is issued first, with an address generator selection in its data field (0 for the source, 1 for the destination). Four PARM commands are then issued, with the coordinates for the rectangular region of memory in the data fields.

PX Command

Command				Data															
3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	X-Coordinate															

2378 Drw 26

Downloads an X-coordinate for the endpoints of a polyline, after an initial endpoint has been downloaded with the LX command. This value is a 13-bit unsigned integer. The value increases from the left to the right of the screen. The PX command is used only for 2-dimensional line drawing, in which I- and Z-values are not required.

Programming Examples

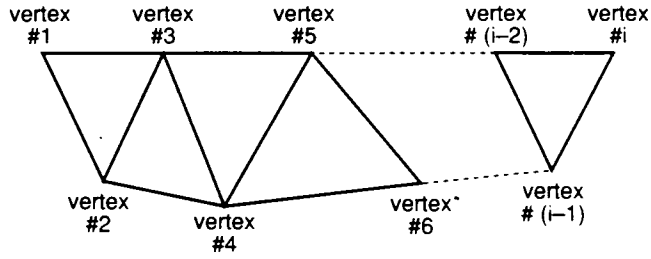
The following sections are examples of command sequences sent to the TC8512. Each example is accompanied by an illustration of the function being executed.

COMMAND	DATA CONTENTS
AUX	PMOD (polygon mode)
PARM	Gouraud Shading (=0)
AUX	ZCNT
PARM	Z Buffer Y/N, Z Section Y/N
I	I value of Vertex #1
Z	Z value of Vertex #1
Y	Y value of Vertex #1
T1X T2X	X value of Vertex #1 for Triangle (Mode 1) X value of Vertex #1 for Triangle (Mode 2)
I	I value of Vertex #2
Z	Z value of Vertex #2
Y	Y value of Vertex #2
X	X value of Vertex #2
.	.
.	.
.	.
I	I value of Vertex #(i–1)
Z	Z value of Vertex #(i–1)
Y	Y value of Vertex #(i–1)
X	X value of Vertex #(i–1)
I	I value of Vertex #i
Z	Z value of Vertex #i
Y	Y value of Vertex #i
X	X value of Vertex #i

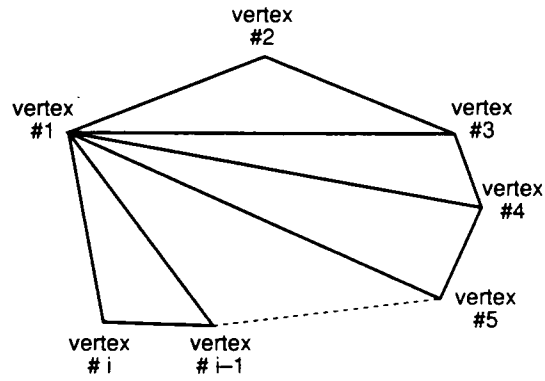
2378 Pgm tbl 15

Triangles with Gouraud Shading

This example shows triangles in which an additional triangle can be defined by downloading an additional vertex. Either a T1X or T2X command may be used, to invoke either of two input modes, as shown below.



(Mode 1)



(Mode 2)

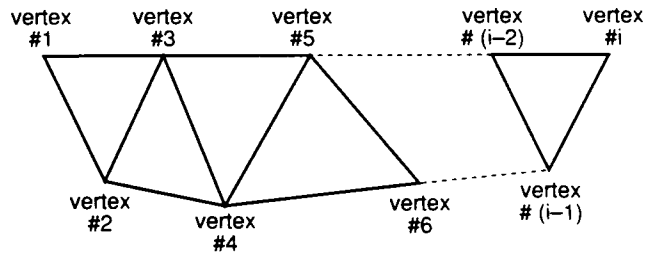
2378 Fhd 15

Triangles with Constant Shading

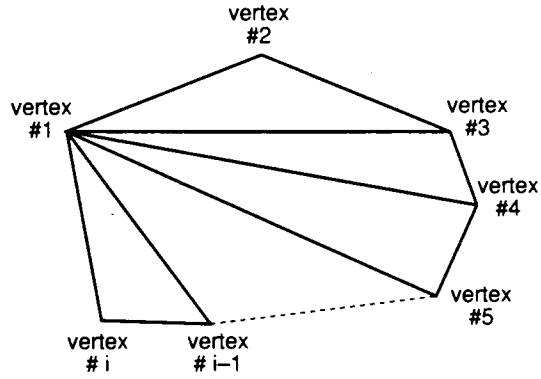
This example shows triangles in which an additional triangle can be defined by downloading an additional vertex. Either a T1X or T2X command may be used, to invoke either of two input modes, as shown below.

COMMAND	DATA CONTENTS
AUX	PMOD (polygon mode)
PARM	Gouraud Shding (=1)
I	I value of Vertex #1
Z	Z value of Vertex #1
Y	Y value of Vertex #1
T1X T2X	X value of Vertex #1 for Triangle (Mode 1) X value of Vertex #1 for Triangle (Mode 2)
Y	Y value of Vertex #2
X	X value of Vertex #2
Y	Y value of Vertex #3
X	X value of Vertex #3
Y	
X	
Y	Y value of Vertex #(i–1)
X	X value of Vertex #(i–1)
Z	Z value of Vertex #i
Y	Y value of Vertex #i
X	X value of Vertex #i

2378 Pgm tbl 16



(Mode 1)



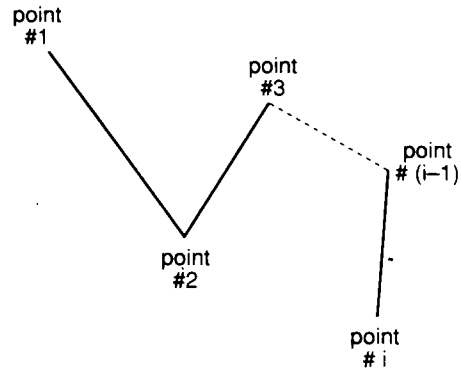
(Mode 2)

2378 Fhd 16

Line Drawing with Depth Cueing

COMMAND	DATA CONTENTS
AUX	LMOD (line drawing mode)
PARM	Depth Cueing (=2)
AUX	ZCNT
PARM	Z Buffer Y/N, Z Section Y/N
.	.
.	.
.	.
I	I value of Point #1
Z	Z value of Point #1
Y	Y value of Point #1
LX	X value of Point #1 for Line Drawing
I	I value of Point #2
Z	Z value of Point #2
Y	Y value of Point #2
X	X value of Point #2
AUX	LSTA (line status)
PARM	Polyline/Separate Line
I	I value of Point #3
Z	Z value of Point #3
Y	Y value of Point #3
X	X value of Point #3
AUX	LSTA (line status)
PARM	Polyline/Separate Line

2378 Pgm tbl 17

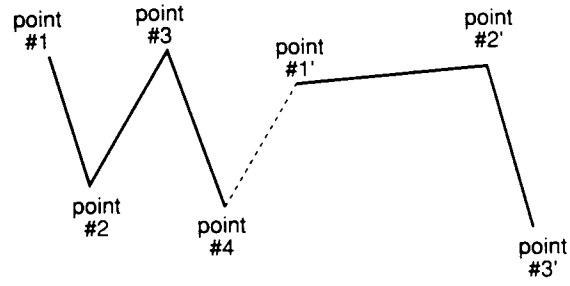


2378 Fhd 17

2-D Line Drawing

COMMAND	DATA CONTENTS
INIT	System Configuration def. CT=0/1
AUX	LMOD (line drawing mode)
PARM	Line (Opaque = 0, Transparent = 1)
.	.
.	.
.	.
Y	Y value of Point #1
LX	X value of Point #1 for Line Drawing
AUX	LSTA (line status)
PARM	Polyline/Separate Line
Y	Y value of Point #2
PX	X value of Point #2
Y	Y value of Point #3
PX	X value of Point #3
AUX	LSTA (line status)
PARM	Polyline/Separate Line
Y	Y value of Point #4
PX	X value of Point #4
Y	Y value of Point #1'
LX	X value of Point #1' for Line Drawing
Y	Y value of Point #2'
PX	X value of Point #2'
Y	Y value of Point #3'
PX	X value of Point #3'

2378 Pgm tbl 18

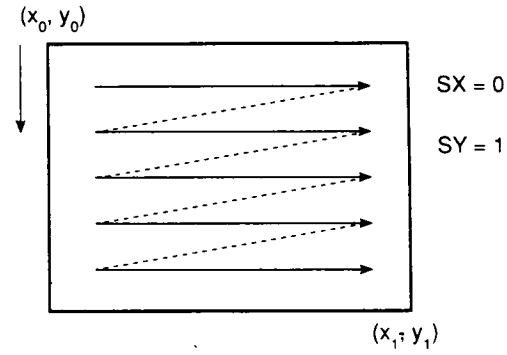


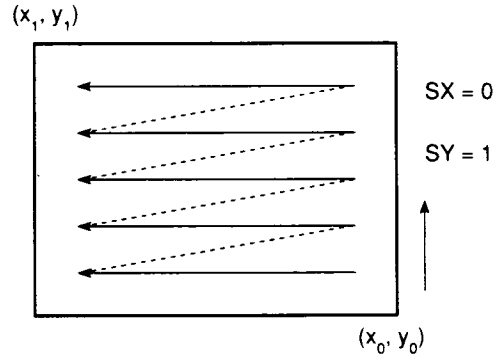
2378 Fhd 18

Image Data Transfer to and from Host Processor

COMMAND	DATA CONTENTS
AUX	LMOD (image Data I/O)
PARM	16 pixel (=0), 1 pixel of 16bit (=1)
AUX	HCNT (Hardware Control Mode)
PARM	Read Modify Write (Y/N)
IMG	Image data I/O, Opaque/Transparent
PARM	Square for Image Out x (x_0)
PARM	Square for Image Out y (y_0)
PARM	Square for Image Out x (x_1)
PARM	Square for Image Out y (y_1)

2378 Pgm tbl 19



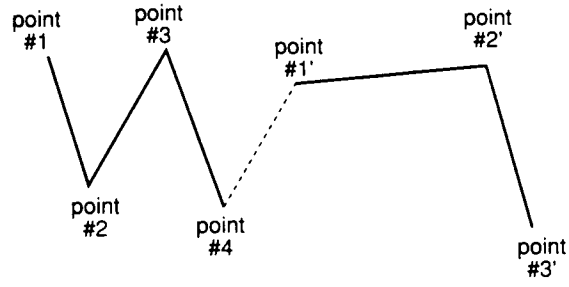


2378 Fhd 19

2-D Line Drawing

COMMAND	DATA CONTENTS
INIT	System Configuration def. CT=0/1
AUX	LMOD (line drawing mode)
PARM	Line (Opaque = 0, Transparent = 1)
.	.
.	.
.	.
Y	Y value of Point #1
LX	X value of Point #1 for Line Drawing
AUX	LSTA (line status)
PARM	Polyline/Separate Line
Y	Y value of Point #2
PX	X value of Point #2
Y	Y value of Point #3
PX	X value of Point #3
AUX	LSTA (line status)
PARM	Polyline/Separate Line
Y	Y value of Point #4
PX	X value of Point #4
Y	Y value of Point #1'
LX	X value of Point #1' for Line Drawing
Y	Y value of Point #2'
PX	X value of Point #2'
Y	Y value of Point #3'
PX	X value of Point #3'

2378 Pgm tbl 18



2378 Fhd 18

Pin Descriptions

Pin Designations

The table shown below matches pin numbers to signal names. Note that different numbers are used for the two package types. All VDD pins must be connected to the +5V power rail. All GND pins must be connected to ground.

Pin No. (PGA)	Pin No. (QFP)	I/O	Signal Name
1	144	3-STATE	$\overline{\text{DTOEI}}$
2	3	O	$\overline{\text{ADGD}}$
3	6	I/O	I15
4	8	I/O	I13
5	11	I/O	I10
6	14	I/O	I7
7	15	I/O	I6
8	17	I/O	I4
9	20	I/O	I3
10	21	I/O	I2
11	25	3-STATE	$\overline{\text{WEZ}}$
12	27	I	ZI15
13	28	I	ZI14
14	32	I	ZI11
15	36	I	ZI7
16	39	I	ZI5
17	42	I	ZI2
18	44	I	ZI0
19	47	I/O	ZO13
20	50	I/O	ZO10
21	51	I/O	ZO9
22	53	I/O	ZO7
23	56	PWR	VDD
24	57	GND	VSS
25	61	I/O	ZO1
26	63	O	$\overline{\text{REQ}}$
27	64	O	$\overline{\text{SYNO}}$
28	67	I/O	$\overline{\text{PYEND}}$
29	72	O	AM
30	75	O	XLEN
31	78	I	$\overline{\text{RESET}}$
32	80	I	$\overline{\text{RDX}}$
33	83	O	IBSY
34	86	I/O	DO
35	87	I/O	D1
36	89	I/O	D3
37	92	I/O	D4
38	93	I/O	D5
39	97	I/O	D9
40	99	I/O	D11
41	100	I/O	D12
42	104	I	A0
43	108	3-STATE	MA25
44	111	3-STATE	MA23
45	114	3-STATE	MA20
46	116	3-STATE	MA18
47	119	3-STATE	MA15
48	122	3-STATE	MA12
49	123	3-STATE	MA11
50	125	PWR	VDD
51	128	3-STATE	MA9
52	129	3-STATE	MA8
53	133	I/O	MA4
54	135	I/O	MA2
55	136	I/O	MA1
56	140	3-STATE	$\overline{\text{CAS}}$
57	143	O	RD/$\overline{\text{WD}}$
58	2	I	WAIT
59	4	O	$\overline{\text{ADGS}}$
60	7	I/O	I14
61	10	I/O	I11
62	12	I/O	I9
63	16	I/O	I5
64	22	I/O	I1
65	23	I/O	I0
66	26	3-STATE	$\overline{\text{WEI}}$
67	29	I	ZI13
68	31	I	ZI12
69	35	I	ZI8
70	38	I	ZI6
71	40	I	ZI4
72	43	I	ZI1

2378 Pgm tbl 23

Pin No. (PGA)	Pin No. (QFP)	I/O	Signal Name
73	46	I/O	ZO14
74	48	I/O	ZO12
75	52	I/O	ZO8
76	58	I/O	ZO4
77	59	I/O	ZO3
78	62	I/O	ZO0
79	65	I	$\overline{SYNI}$
80	67	I/O	$\overline{PXEND}$
81	71	O	XFR
82	74	O	XREN
83	76	O	YTEN
84	79	I	TEST
85	82	I	$\overline{WDX}$
86	84	O	NFLL
87	88	I/O	D2
88	94	I/O	D6
89	95	I/O	D7
90	98	I/O	D10
91	101	I/O	D13
92	103	I/O	D15
93	107	I	A3
94	110	3-STATE	MA24
95	112	3-STATE	MA22
96	115	3-STATE	MA19
97	118	3-STATE	MA16
98	120	3-STATE	MA14
99	124	GND	VSS
100	130	3-STATE	MA7
101	131	3-STATE	MA6
102	134	I/O	MA3
103	137	I/O	MA0
104	139	3-STATE	$\overline{RAS}$
105	142	O	SC
106	1	GND	VSS
107	5	O	FAST
108	9	I/O	I12

Pin No. (PGA)	Pin No. (QFP)	I/O	Signal Name
109	13	I/O	I8
110	18	PWR	VDD
111	19	GND	VSS
112	24	3-STATE	$\overline{WEZS}$
113	30	PWR	VDD
114	33	I	ZI10
115	34	I	ZI9
116	37	GND	VSS
117	41	I	ZI3
118	45	I/O	ZO15
119	49	I/O	ZO11
120	54	I/O	ZO6
121	55	I/O	ZO5
122	60	I/O	ZO2
123	66	O	M/$\overline{I}$
124	69	O	$\overline{SRTP}$
125	70	I/O	B/$\overline{P}$
126	73	GND	VSS
127	77	O	YBEN
128	81	PWR	VDD
129	85	O	CBSY
130	90	GND	VSS
131	91	PWR	VDD
132	96	I/O	D8
133	102	I/O	D14
134	105	I	A1
135	106	I	A2
136	109	PWR	VDD
137	113	3-STATE	MA21
138	117	3-STATE	MA17
139	121	3-STATE	MA13
140	126	I	CLK
141	127	3-STATE	MA10
142	132	I/O	MA5
143	138	O	OEACK
144	141	3-STATE	$\overline{DTOEZ}$

2378 Pgm tbl 23

Signal Descriptions

The signals on the TC8512 comprise five main groups: host interface, VRAM interface, interchip synchronization (only used for multiple TC8512s), memory access modes, and fill control signals.

Host Interface

These signals are the interface between the TC8512 and the host system. Typically, they connect to either the processor's bus or an expansion bus, such as NuBus or Micro Channel.

Symbol	Name	I/O	Description
D0-D15	Data Bus	I/O	Bidirectional 16-bit bus between the host processor and the TC8512. It is an input when commands are downloaded from the processor, and it is an output when the host processor reads data from VRAM.
A0-A3	Address Bus	I	Receives commands from the host processor. When used with a bus that has byte addressing, these typically will be connected to the address lines just above the lowest address bit (i.e., A0-A3).
$\overline{WDX}$	Write Data Strobe	I	Loads D0-D15 and A0-A3 into the TC8512. These signals may be pushed into the command FIFO or passed through to VRAM. This signal is synchronized internally, and it is active low.
$\overline{RDX}$	Read Data Strobe	I	Asserted by the host processor to read from the I-buffer. This signal is synchronized internally, and it is active low.
TEST	Test Mode Enable	I	Enables a test mode used by the manufacturer. Must be tied low.
CBSY	Channel Busy	O	Indicates the TC8512 is busy. Any operation, such as filling a triangle, will assert this signal, even if the command FIFO is empty. Any pending operation, such as any command waiting in the FIFO, will also cause the assertion of this signal. This signal is active high.
NFLL	Not Full	O	Indicates whether there is room in the command FIFO to accept another command. This signal is active high.
IBSY	Image Data Busy	O	Synchronous signal at image input or output: 1 = The TC8512 is reading image data from or writing image data to VRAM. The host processor must wait during this period. 0 = The TC8512 has finished reading or writing image data and is ready for the next data transfer.

Symbol	Name	I/O	Description
CLK	Clock	I	A 50% duty-cycle clock signal. Any clock rate from DC to 12 MHz may be used.
$\overline{\text{RESET}}$	Reset	I	Initializes the TC8512. It only needs to be asserted for one clock period. This signal is synchronized internally, and it is active low.

VRAM Interface

These signals comprise the interface to the random-access and serial ports of VRAM. The random-access port is like the interface to ordinary DRAM. The serial port is like a shift register.

Symbol	Name	I/O	Description
$\overline{\text{RAS}}$	Row Address Strobe	O, 3-state	Drives the RAS signal. Typically, buffering will be required. This signal is active low.
$\overline{\text{CAS}}$	Column Address Strobe	O, 3-state	Used to develop the CAS signals in external circuits. The timing of this signal precedes the timing of the CAS applied to the VRAMs by one clock period. This signal is active low.
XFR	Transfer	O	Indicates the TC8512 is reading from the serial port of the Z-buffer VRAM. This signal is active high.
$\overline{\text{DTOEI}}$	Data Transfer/Output Enable, I-Buffer	O, 3-state	Enables the shift register transfer cycle for the I-buffer. It is asserted on the falling edge of RAS. It is not asserted while old Z-coordinates are being read into the TC8512. This signal is active low.
$\overline{\text{DTOEZ}}$	Data Transfer/Output Enable, Z-Buffer	O, 3-state	Enables the shift register transfer cycle for the Z-buffer. It is asserted on the falling edge of RAS, while old Z-coordinates are being read into the TC8512. This signal is active low.
SC	Serial Clock	O	Clock signal for shifting Z-coordinates out of the serial port.
RD/$\overline{\text{WD}}$	Read/Write	O	Output which indicates whether the TC8512 is reading or writing through the random-access port of VRAM. Low indicates writing; high indicates reading.

Symbol	Name	I/O	Description
$\overline{ADGD}$	Address Generator Destination	O	Selects whether memory should be addressed by the source or destination chip (only used in the two-chip address generator mode). Low selects the destination chip; high selects the source chip.
$\overline{ADGS}$	Address Generator Source	O	Indicates whether the TC8512 is the source chip (only used in address generator mode). This signal is active low.
FAST	Fast Mode	O	Indicates whether the TC8512 is in 16-pixel mode (only used with constant shading). This signal is active high.
$\overline{WEI}$	Write Enable, I-Buffer	O, 3-State	Enables write cycles to the I-buffer. This signal is active low.
$\overline{WEZ}$	Write Enable, Z-Buffer	O, 3-State	Enables write cycles to the Z-buffer. This signal is active low.
$\overline{WEZS}$	Write Enable, Z-Sectioning Buffer	O, 3-State	Enables write cycles to the Z-sectioning buffer. This signal is active low.
M/$\bar{I}$	Mask/Index	O	Indicates the multiplexing of the I- and Z-buses. When using the 16-pixel mode (only used with constant shading), low indicates output of an I-value on the I-bus; high indicates output of a 16-pixel mask on the I-bus. This output assumes a different meaning when uploading the Z- and Z-sectioning buffers to the host processor. High selects the Z-sectioning buffer; low selects the Z-buffer.
I15-I0	Color Intensity	I/O 3-State	Bidirectional bus for I-values. This bus is connected to the random-access port of the I-buffer VRAM. During drawing operations, I-values are loaded to the I-buffer through this bus. In 16-pixel mode (only used for constant shading), the I-values are multiplexed with 16-pixel bit masks. This bus becomes an input when the I-buffer is uploaded to the host processor.

Symbol	Name	I/O	Description
ZO15-ZO0	Z Output	I/O, 3-State	Bidirectional bus for new Z-coordinates. This bus is connected to the random-access port of the Z-buffer VRAM. During drawing operations, Z-coordinates are loaded to the Z-buffer through this bus. This bus becomes an input when the Z-buffer is uploaded to the host processor.
ZI15-ZI0	Z Input	I	Input bus for old Z-coordinates. This bus is connected to the serial port of the Z-buffer VRAM. The timing of this bus is delayed from the Z-output bus by two clock periods, to allow pipelining of the Z-comparison. When Z-sectioning is used, this bus is multiplexed between the Z-buffer and the Z-sectioning buffer.
MA25-MA0	Memory Address	O, 3-State	Output bus for addressing VRAM. Depending on the mode, it can be either two 13-bit addresses (representing X and Y), or one linear address. Address multiplexing must be performed externally.
WAIT	Wait	I	Input which pauses the TC8512, and causes it to float the following signals: MA25-MA0, $\overline{RAS}$, $\overline{CAS}$, $\overline{DTOEI}$, $\overline{DTOEZ}$, ZO15-ZO0, I15-I0, $\overline{WEI}$, $\overline{WEZ}$, and $\overline{WEZS}$. This signal is active high.
OEACK	Output Enable Acknowledge	O	Output which indicates when the TC8512 has floated its bus in response to assertion of WAIT. This signal is active high.

Interchip Synchronization

These signals are used for multichip configurations, which can be either two or four staggered chips for increased drawing rates, two chips for increased I-width (used for RGB color), or the two-chip address generator configuration.

Symbol	Name	I/O	Description
$\overline{\text{SYNO}}$	Sync Out	O	In polygon shading mode, there is a certain amount of calculation overhead before the TC8512 is ready to begin drawing. To allow multiple chips to begin shading at the same time, this output goes low when a TC8512 is ready to draw. The $\overline{\text{SYNO}}$ outputs from all chips are ORed together, and the resulting signal is applied to all $\overline{\text{SYNI}}$ inputs. In the two-chip address generator mode, the $\overline{\text{SYNO}}$ output from the source chip indicates when a read cycle has been completed. This connects to the $\overline{\text{SYNI}}$ input of the destination chip to trigger a write cycle. When the destination chip has completed its write cycle, its $\overline{\text{SYNO}}$ output goes low, which is returned to the source chip on its $\overline{\text{SYNI}}$ input.
$\overline{\text{SYNI}}$	Sync In	I	See above description of the $\overline{\text{SYNO}}$ signal.
$\overline{\text{PXEND}}$	Pixel X End	I/O	Indicates when a TC8512 has reached the last pixel of a horizontal scan (only used in the two-chip address generator mode).
$\overline{\text{PYEND}}$	Pixel Y End	I/O	Indicates when a TC8512 has reached the last line of a vertical scan (only used in the two-chip address generator mode).

Memory Access Mode

These signals indicate the mode settings for access to memory. They can be used to implement a flexible configuration in the external circuitry. For example, fast constant shading in 16-pixel mode can be used to initialize the I- and Z-buffers prior to Gouraud shading.

Symbol	Name	I/O	Description
B/$\overline{P}$	Block/Pixel	O	Indicates whether 16-pixel mode is being used (constant shading only). High indicates 16-pixel mode; low indicates single pixel block mode.
AM	Addressing Mode	O	Indicates whether the internal pixel cache is organized as 4 x 4 or 16 x 1.

Fill Control Signals

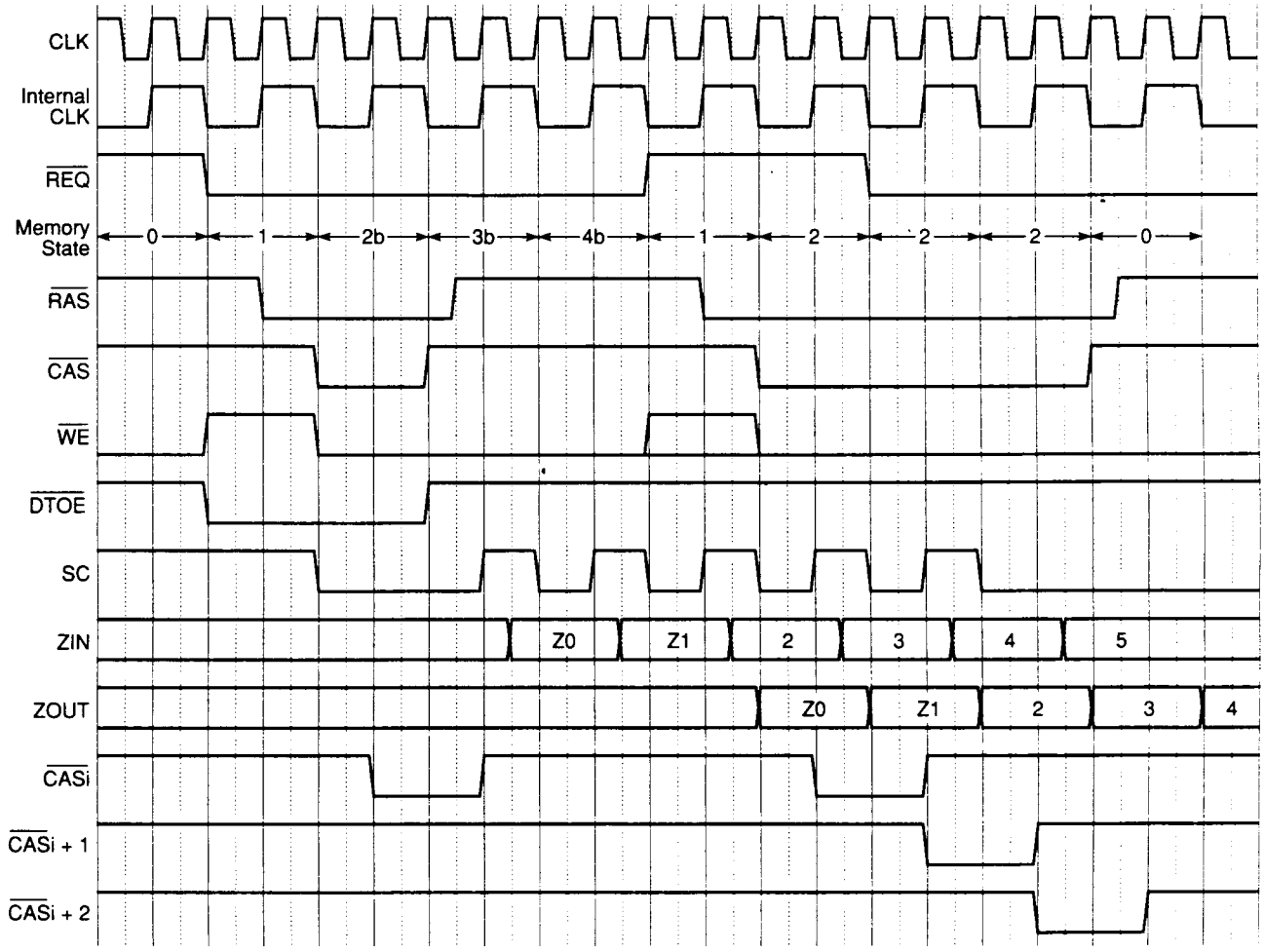
These signals indicate the direction of the scanning process which generates new I- and Z-values.

Symbol	Name	I/O	Description
$\overline{REQ}$	Memory Request	O	Indicates access to VRAM. This signal is asserted two clock periods before the first DRAM access, and it is active low.
$\overline{SRTP}$	S44	O	Indicates access to the first pixel of a polygon fill. This signal is active low.
XLEN	X Left Enable	O	Indicates the scan has moved to the left. This signal is active high.
XREN	X Right Enable	O	Indicates the scan has moved to the right. This signal is active high.
YTEN	Y Top Enable	O	Indicates the scan has moved up. This signal is active high.
YBEN	Y Bottom Enable	O	Indicates the scan has moved down. This signal is active high.

Timing Diagrams

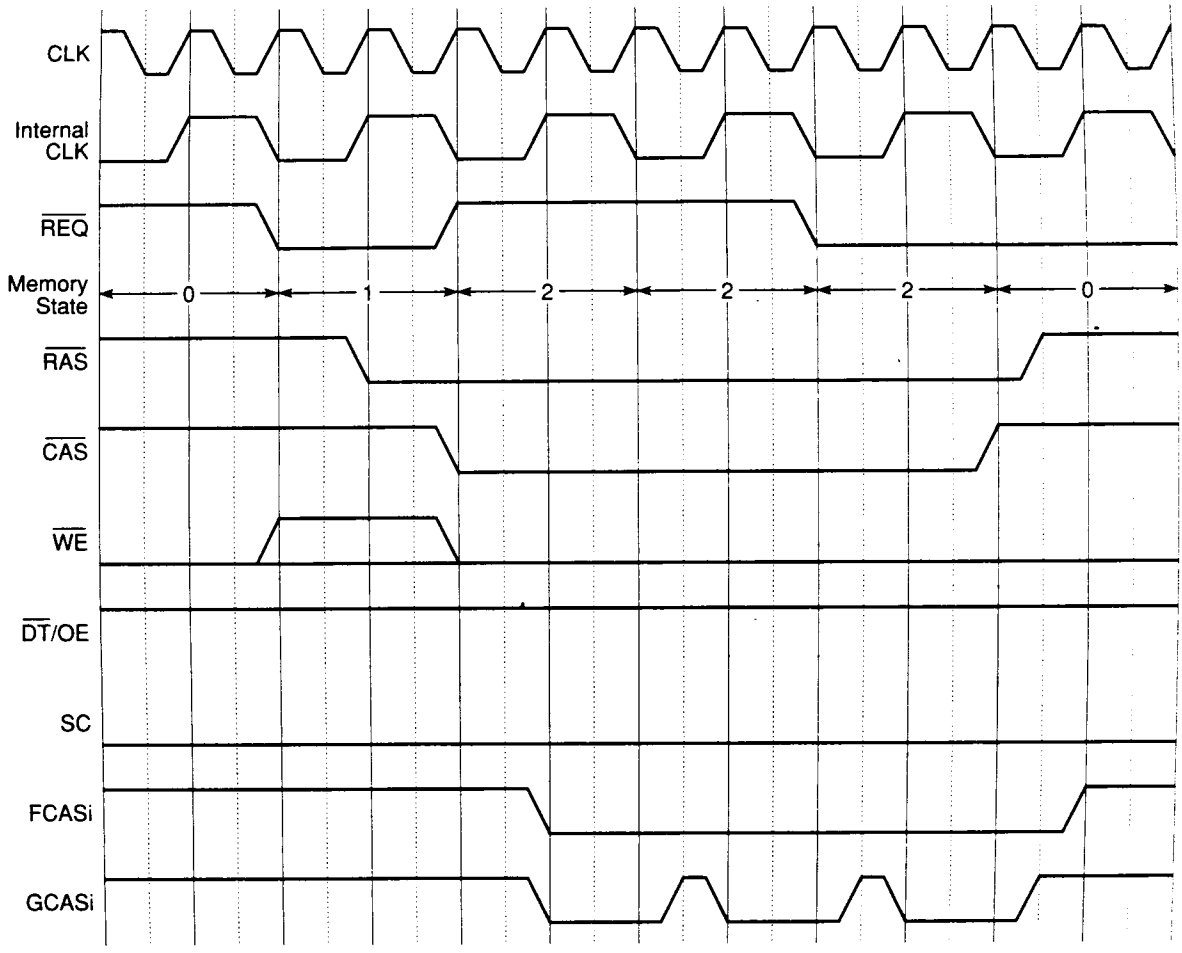
The following diagrams show typical operations performed by the TC8512. The CAS signals must be generated in external logic. These signals are shown with an "i" suffix, as in CASi, CASi+1, FCASi, etc.

Gouraud Shading



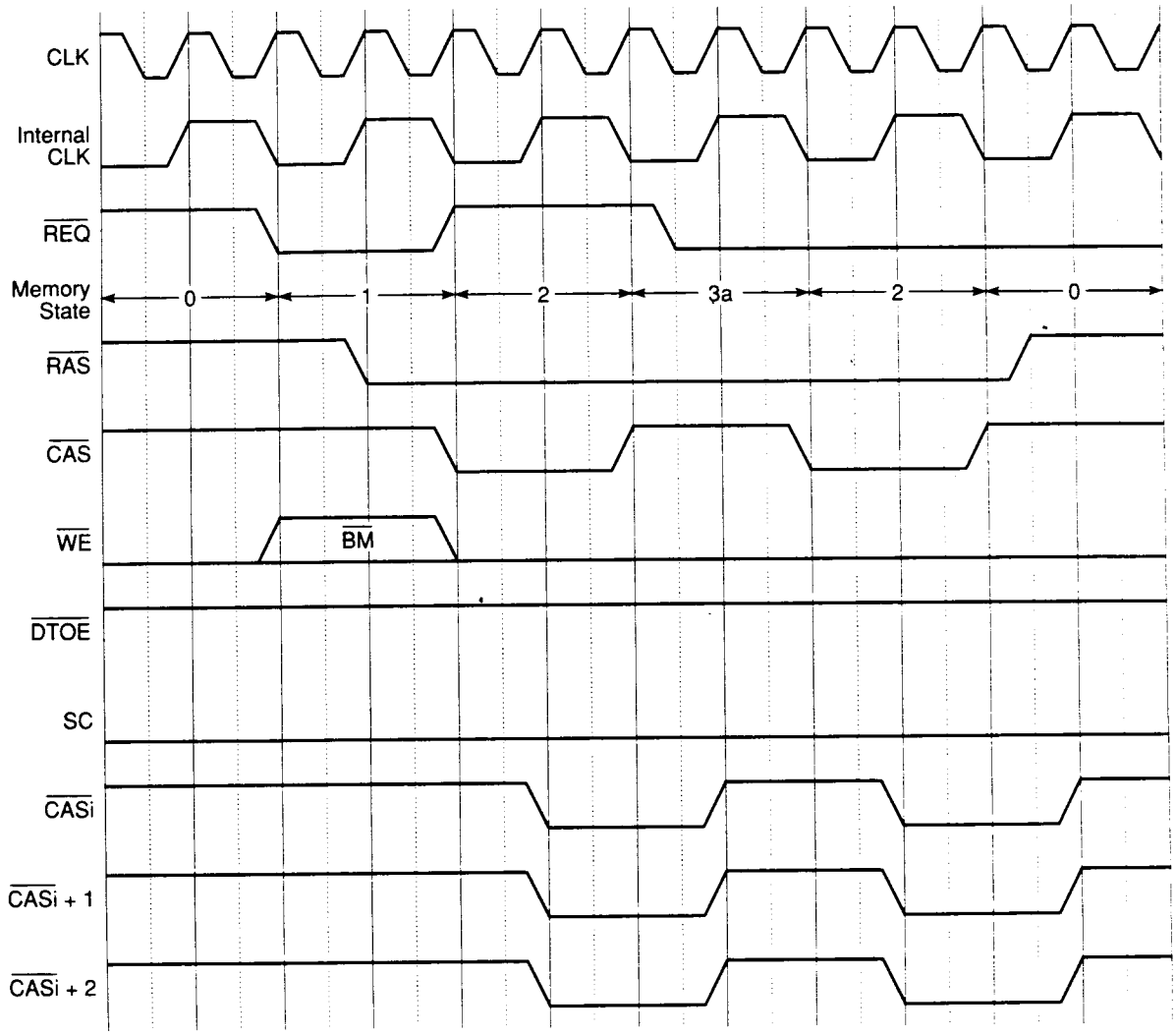
2378 Fhd 24a

Page Write (Constant Shading, Long $\overline{CAS}$)



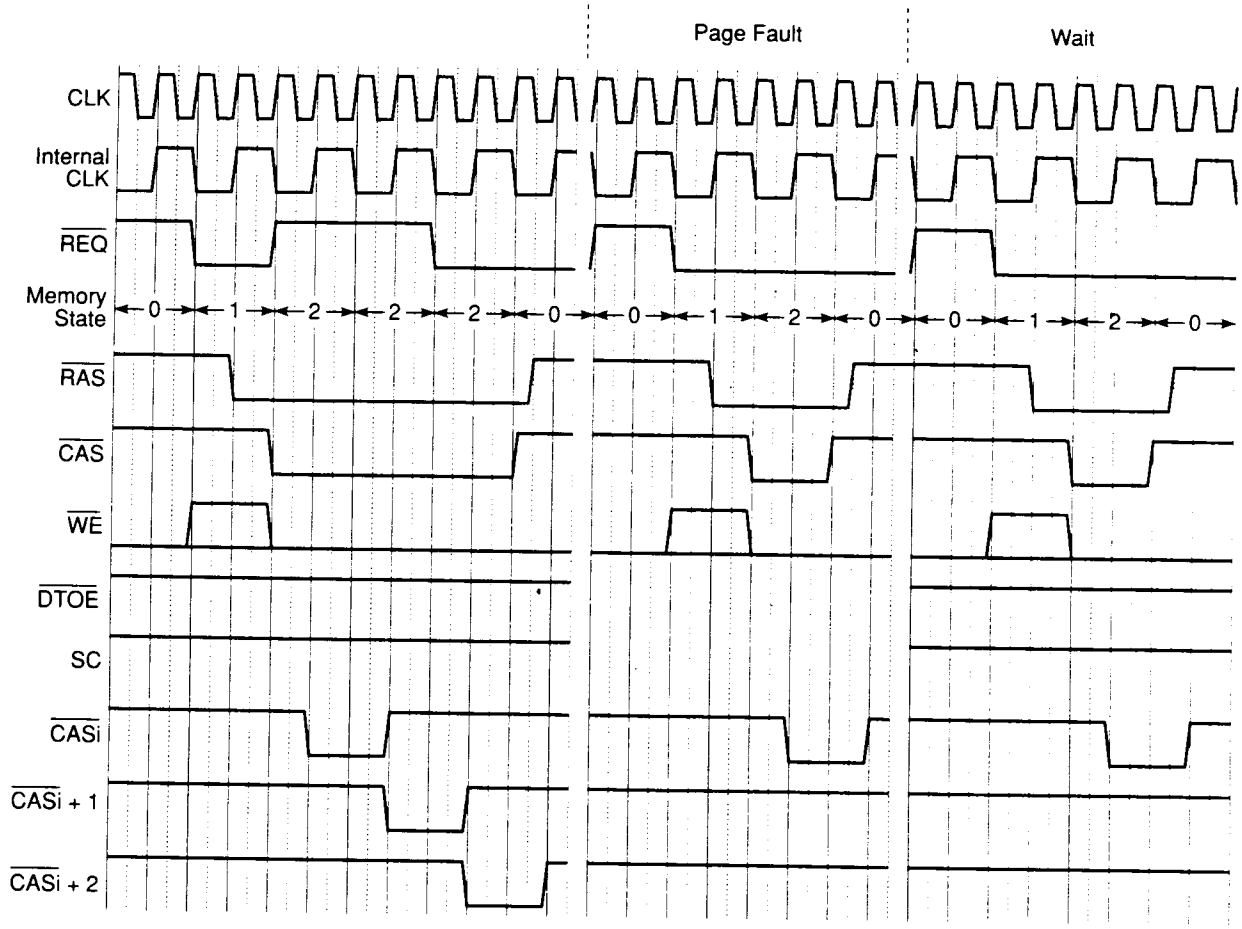
2378 Fhd 24b

Page Write (Constant Shading, Short $\overline{CAS}$)



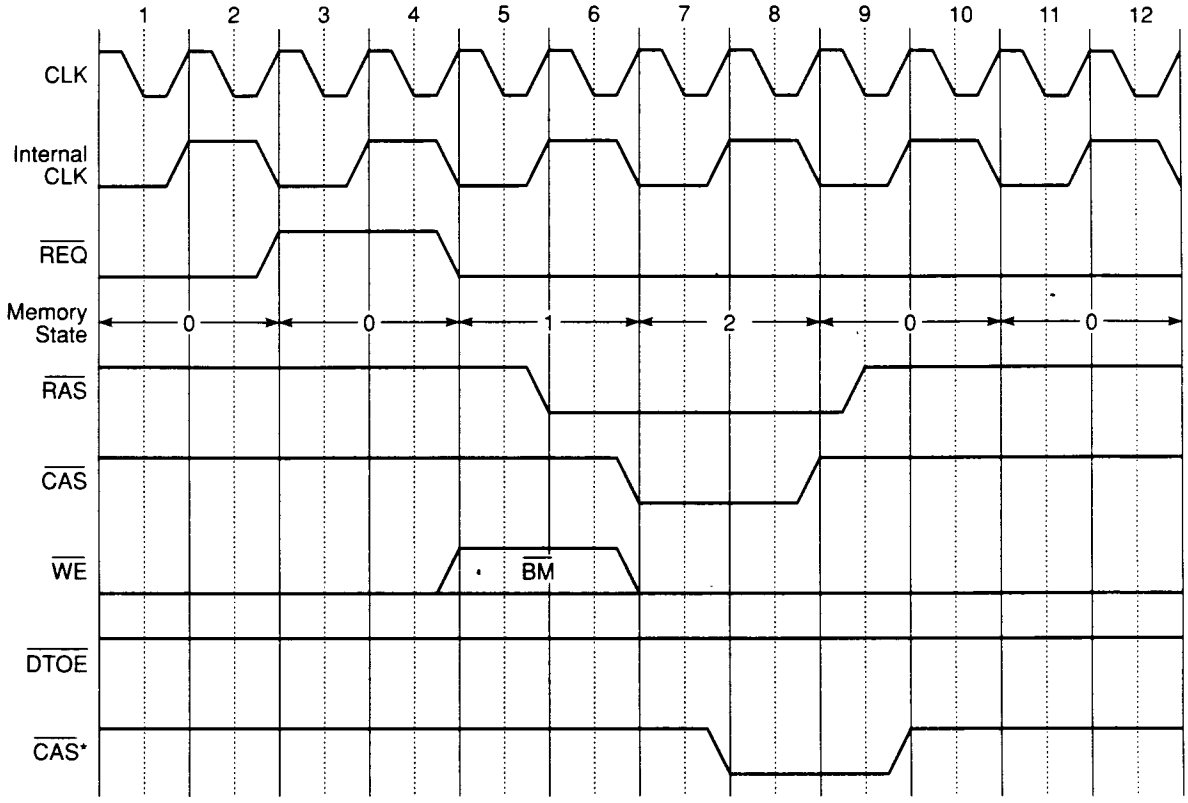
2378 Fhd 24c

Page Write (Gouraud Shading)



2478 Fhd 24d

Line Drawing (Pixel Write)



2378 Fhd 24e

Line Drawing (Cache)

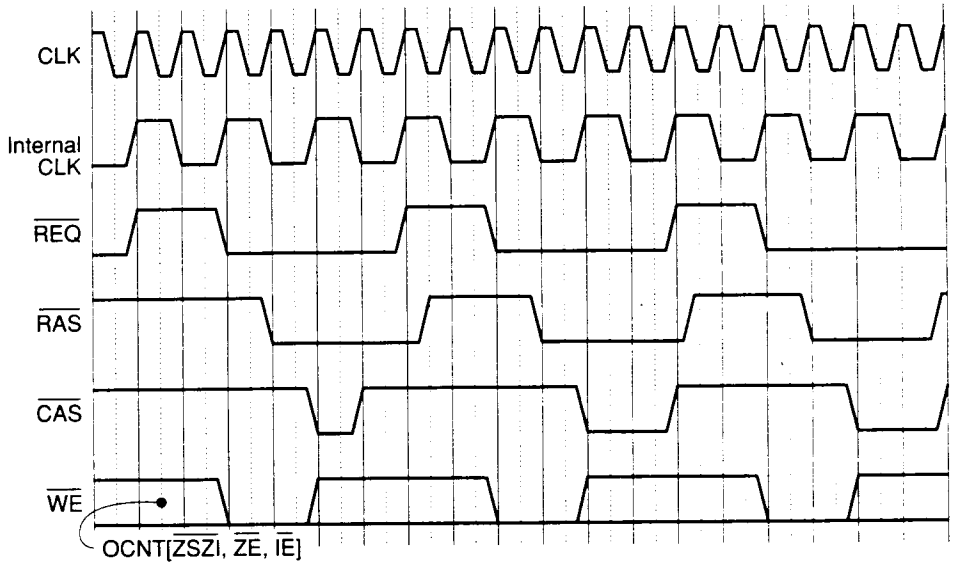
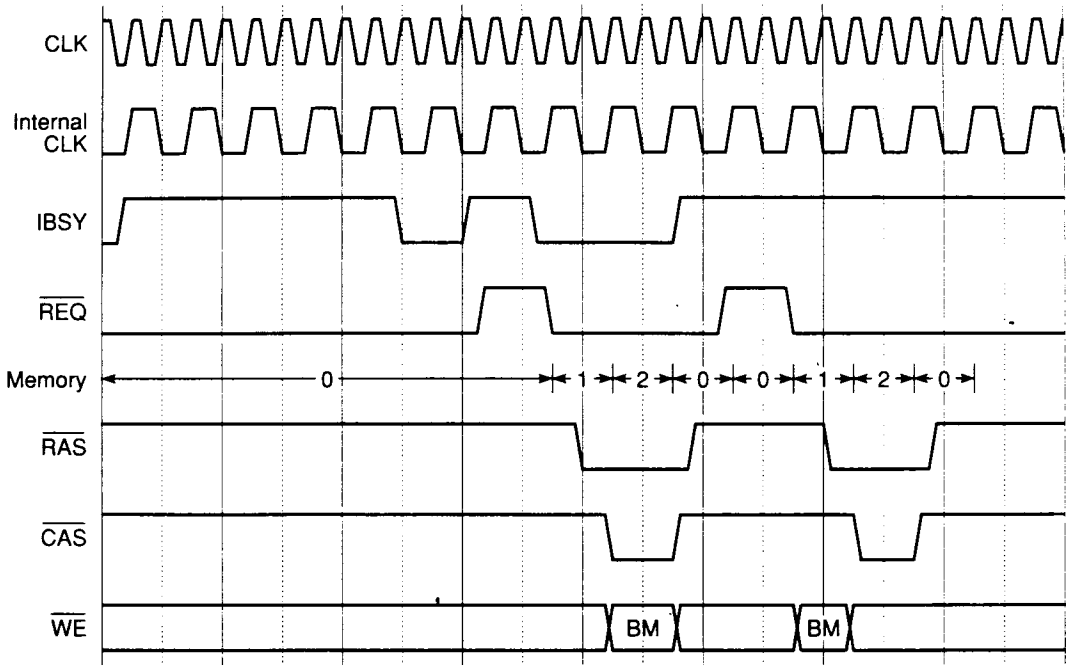
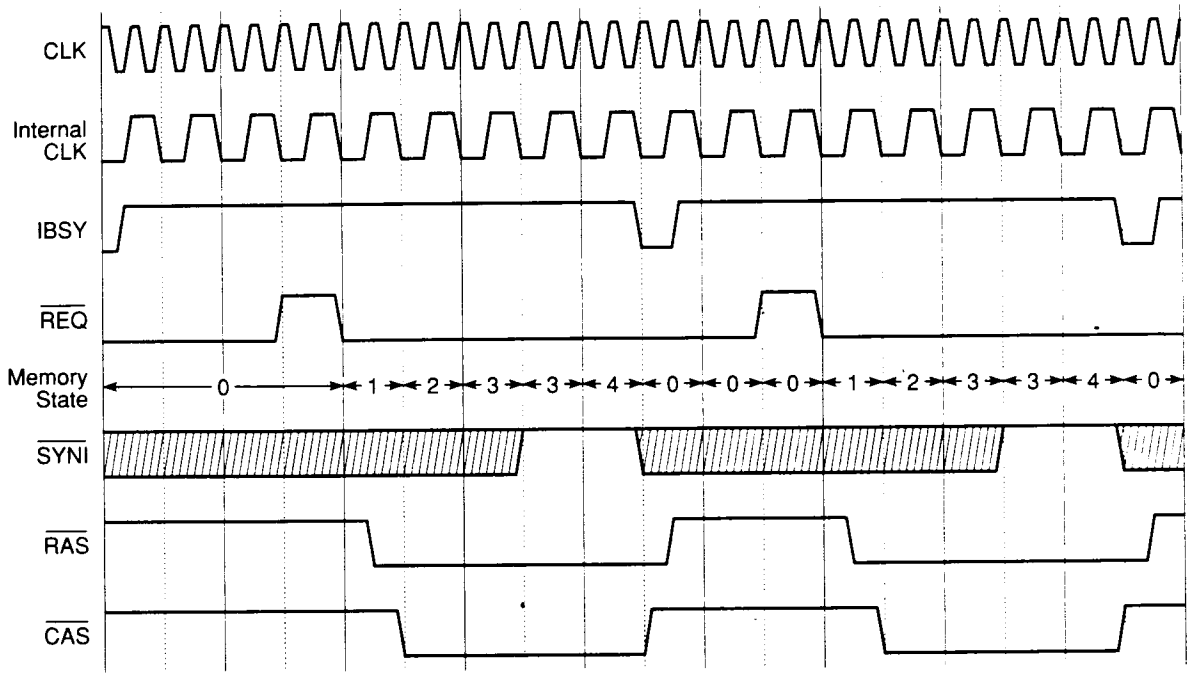


Image Out



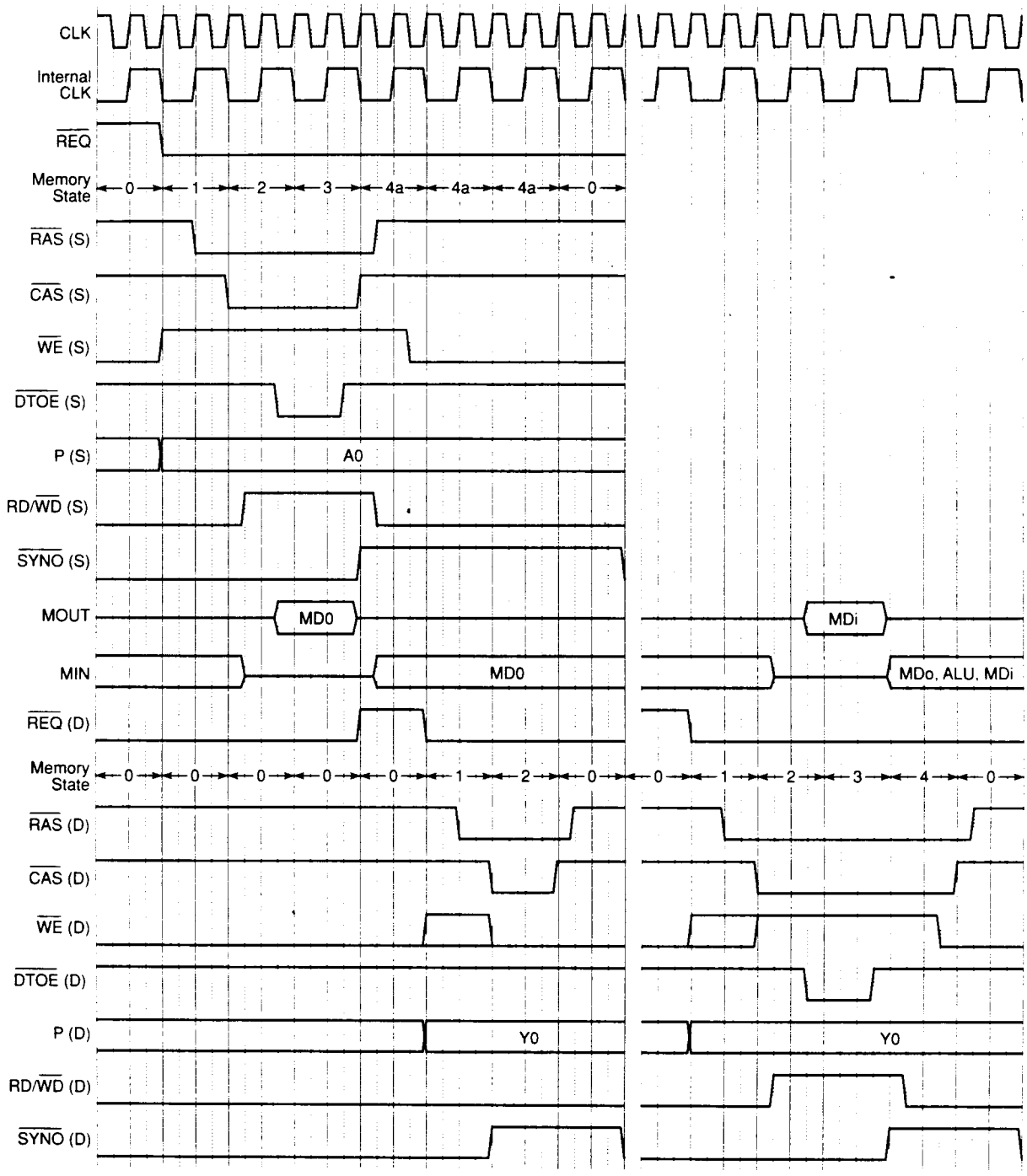
2378 Fhd 24g

Image In



2378 Fhd 24h

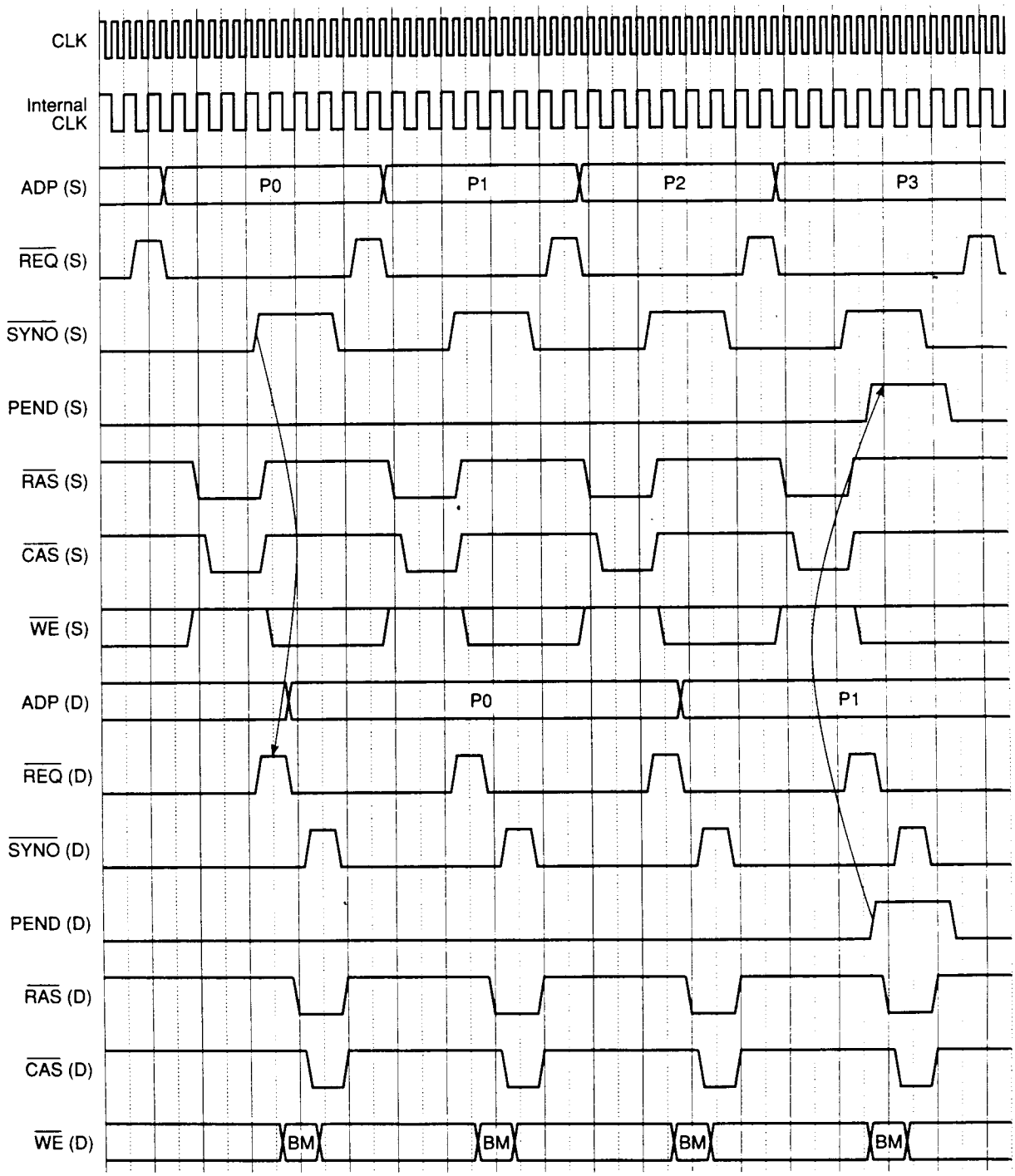
Address Generator (Source and Destination)



(S) = Source
(D) = Destination

2378 Fhd 24

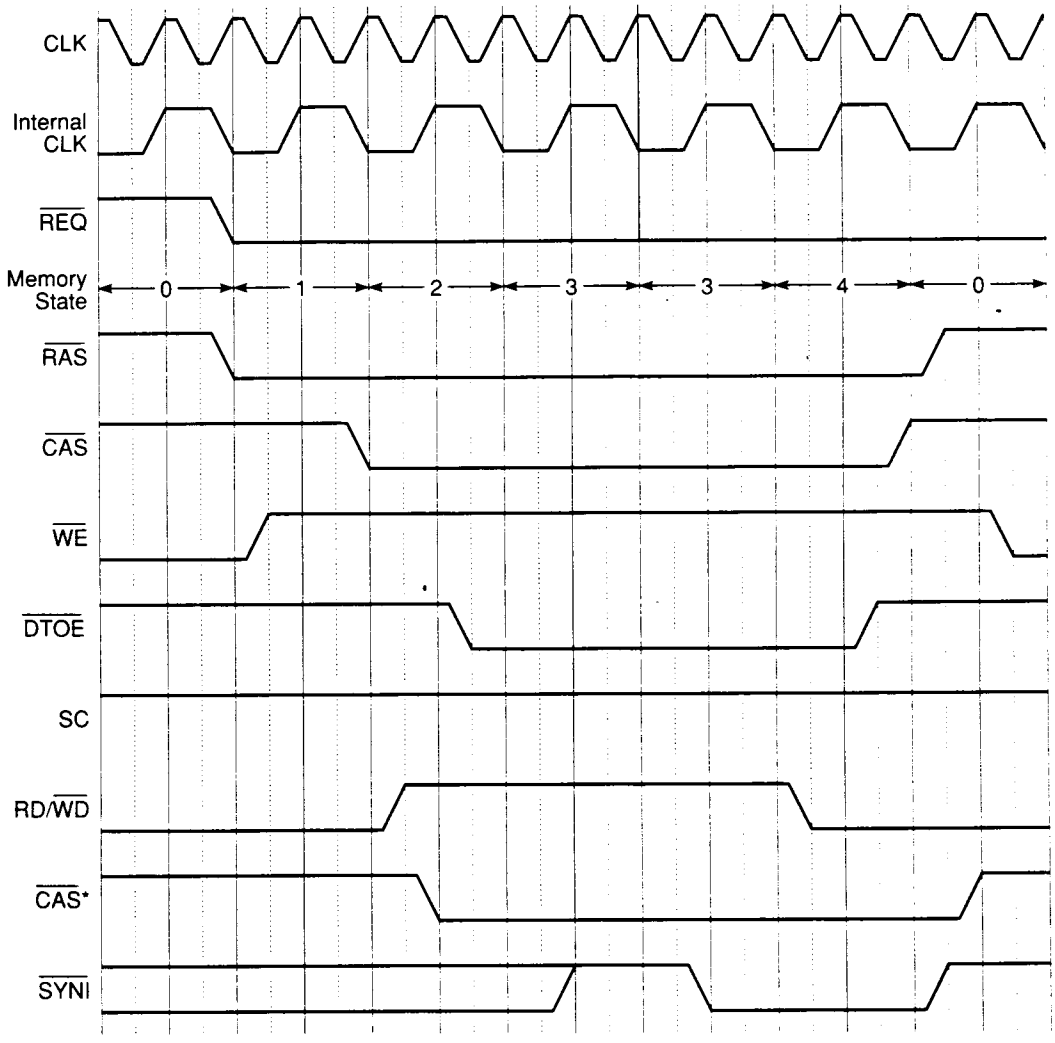
Address Generator Scaling (Source and Destination)



(S) = Source
(D) = Destination

2378 Fhd 24j

Read Mode (CPU)



2378 Fhd 24k

Absolute Maximum Ratings

V_{ss} = 0V (GND)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	–0.5 ~ +7.0	V
Input Voltage	V_{IN}	–0.3 ~ +7.0	V
Operating Temperature	T_{OPR}	0 ~ +70	°C
Storage Temperature	T_{STG}	–65 ~ +125	°C

2378 Pgm tbl 25

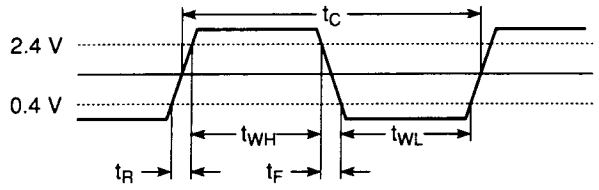
DC Specifications

T_a = 0°C~70°C, V_{SS} = 0V, V_{DD} = 5V±5%

PARAMETER	SYMBOL	CONDITION	MIN.		MAX.		UNIT
			12 MHz	16 MHz	12 MHz	16 MHz	
Input Low Voltage	V_{IL}		0	0	0.8	0.4	V
Input High Voltage	V_{IH}		2.2	2.2	V_{DD}	V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA	–	–	0.4	0.4	V
Output High Voltage	V_{OH}	I_{OH} = –0.4mA	2.4	2.4	–	–	V
Power Supply Current	I_{DD}		–	–	200	200	mA
Input Leakage Current	I_{LI}		–	–	±10	±10	µA
Output Leakage Current	I_{LO}		–	–	±10	±10	µA
Input Low Voltage	V_{IL} (CLK)		0	0	0.4	0.4	V
Input High Voltage	V_{IH} (CLK)		3.6	3.6	V_{DD}	V_{DD}	V
Capacitance of Input Buffer	C_{IN}		–	–	10	10	pF

2378 Pgm tbl 26

AC Characteristics



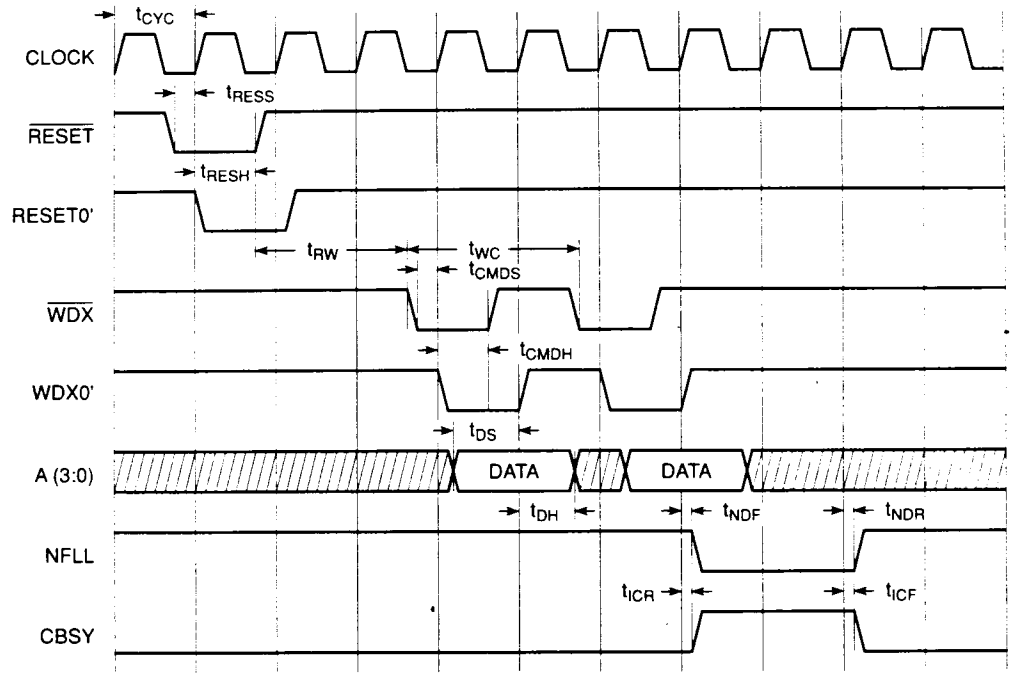
2378 Fhd 27a

PARAMETER	SYMBOL	MIN.		MAX.		UNIT
		12 MHz	16 MHz	12 MHz	16 MHz	
Cycle Time	t_C	83	62.5	–	–	ns
Rise Time	t_R	–	–	5	5	ns
Fall Time	t_F	–	–	5	5	ns
H-level Pulse Width	t_{WH}	36	26	–	–	ns
L-level Pulse Width	t_{WL}	36	26	–	–	ns

2378 Pgm tbl 27a

AC Specifications

Host Interface and Clock Timing



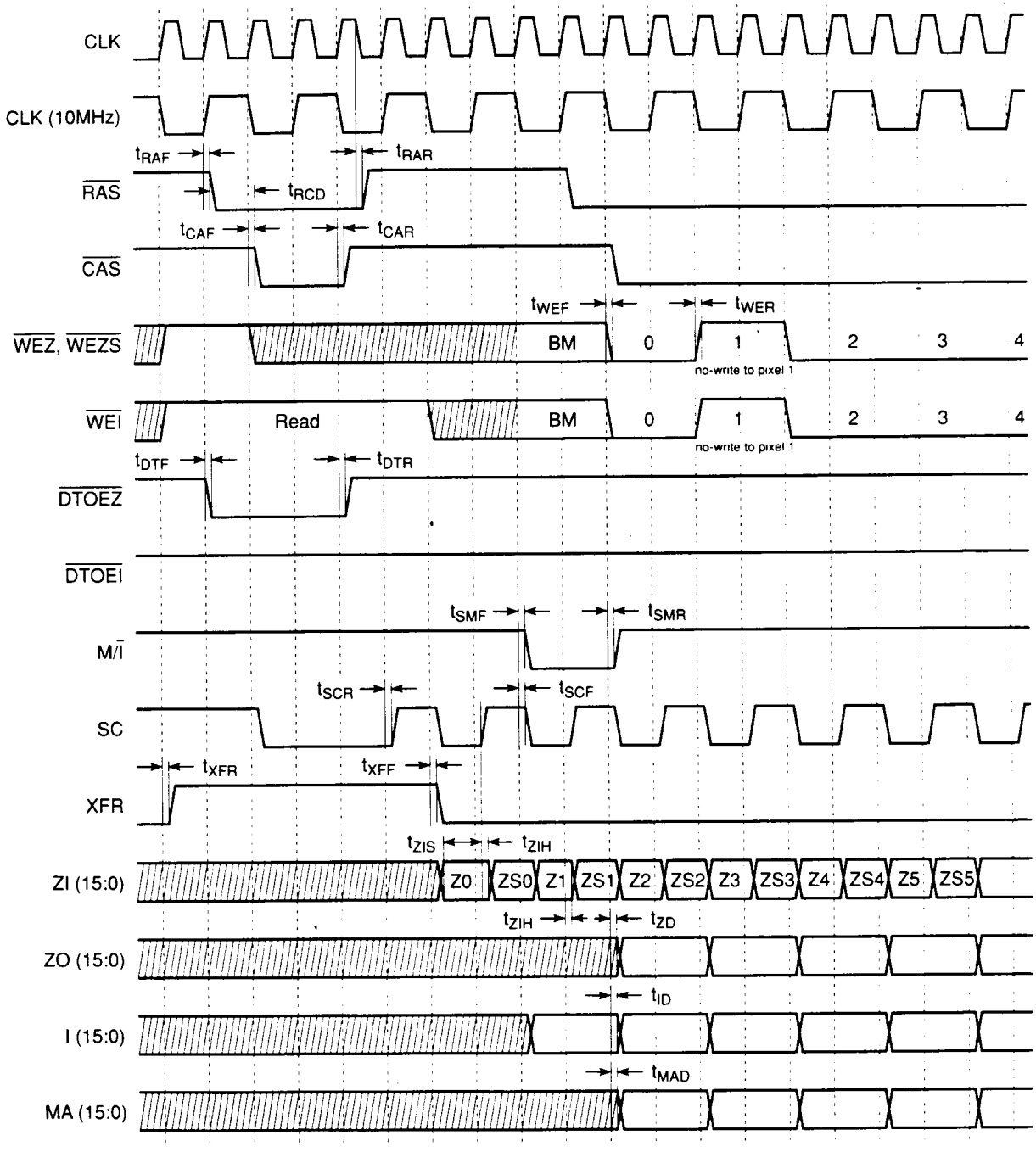
The diagram illustrates the command input mode.
RESET0' and WDX0' are internally synchronized.

2378 Fhd 27B

T_a = 0°C~70°C, V_{SS} = 0V, V_{DD} = 5V±5%, C_L = 60pF

PARAMETER	SYMBOL	CONDITION	MIN.		MAX.		UNIT
			12 MHz	16 MHz	12 MHz	16 MHz	
Clock Cycle Period	t_{CYC}		83	62.5	—	—	ns
$\overline{RESET}$ Setup Time	t_{RESS}		5	5	—	—	ns
$\overline{RESET}$ Hold Time	t_{RESH}		20	20	—	—	ns
$\overline{RESET}$ to $\overline{WDX}$ Delay Time	t_{RW}		$2t_{CYC}$	$2t_{CYC}$	—	—	ns
$\overline{WDX}$ Cycle Time	t_{WC}		$2t_{CYC}$	$2t_{CYC}$	—	—	ns
$\overline{WDX}$, $\overline{RDX}$ Setup Time	t_{CMDS}		5	NA	—	—	ns
$\overline{WDX}$, $\overline{RDX}$ Hold Time	t_{CMDH}		10	NA	—	—	ns
Data, A Setup Time	t_{DS}		5	20	—	—	ns
Data, A Hold Time	t_{DH}		20	10	—	—	ns
NFLL Active Delay	t_{NDF}		—	—	50	50	ns
NFLL Inactive Delay	t_{NDR}		—	—	50	50	ns
IBSY, CBSY Active Delay	t_{ICR}		—	—	50	50	ns
IBSY, CBSY Inactive Delay	t_{ICF}		—	—	50	50	ns
$\overline{WDX}$ Pulse Width	t_{WPW}		—	50	—	—	ns

Serial Read and Page Write

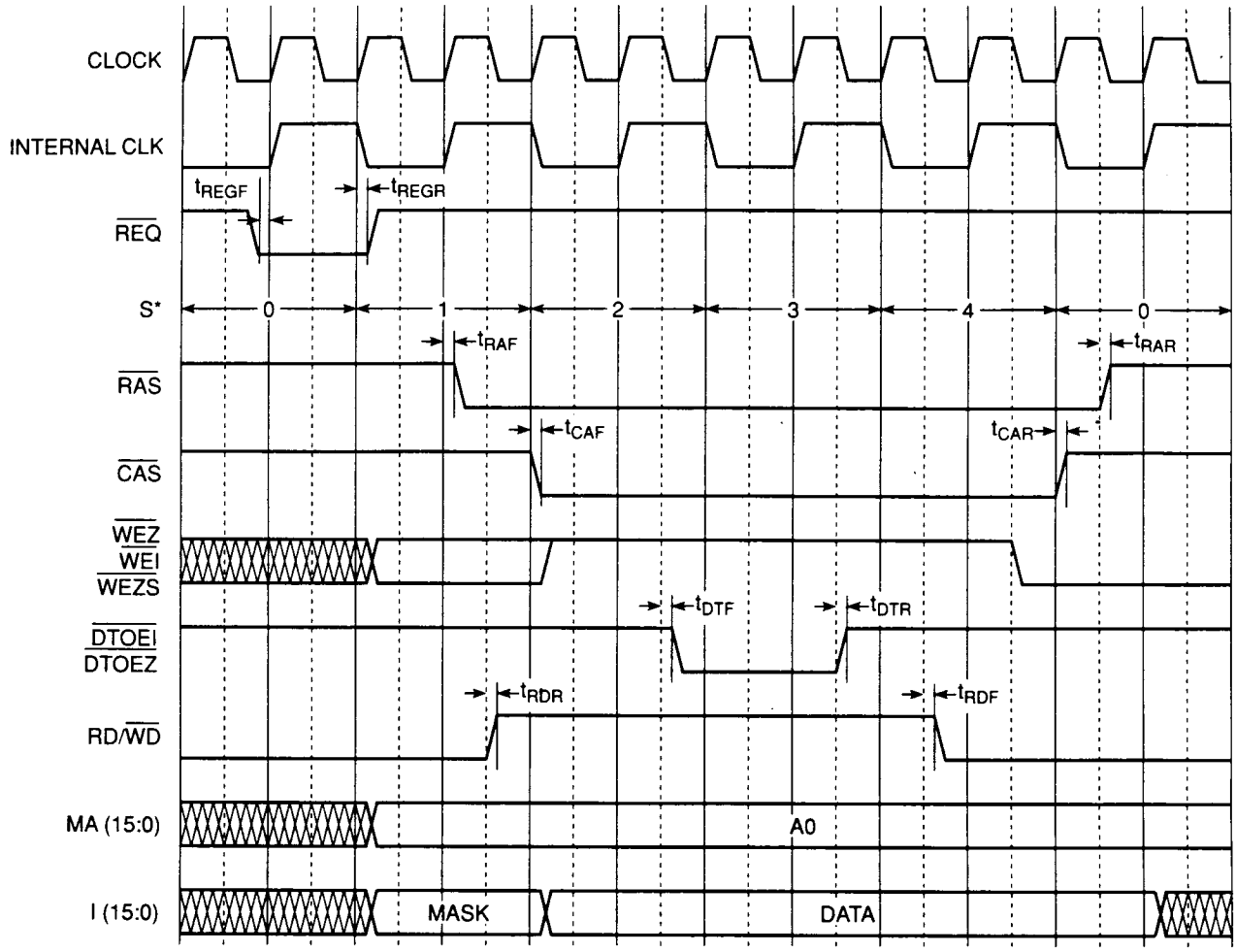


2378 Fhd 27d

PARAMETER	SYMBOL	CONDITION	MIN.		MAX.		UNIT
			12 MHz	16 MHz	12 MHz	16 MHz	
$\overline{RAS}$ Active Delay	t_{RAF}		10	5	40	40	ns
$\overline{RAS}$ Inactive Delay	t_{RAR}		10	5	40	40	ns
$\overline{CAS}$ Active Delay	t_{CAF}		10	5	40	40	ns
$\overline{CAS}$ Inactive Delay	t_{CAR}		10	5	40	40	ns
$\overline{WEI}$, $\overline{WEZ}$, $\overline{WEZS}$, Active Delay	t_{WEF}		—	—	50	50	ns
$\overline{WEI}$, $\overline{WEZ}$, $\overline{WEZS}$, Inactive Delay	t_{WER}		—	—	50	50	ns
$\overline{DTOEI}$, $\overline{DTOEZ}$, Active Delay	t_{DTF}		—	—	50	50	ns
$\overline{DTOEI}$, $\overline{DTOEZ}$, Inactive Delay	t_{DTR}		—	—	50	50	ns
SC Active Delay	t_{SCR}		—	—	40	40	ns
SC Inactive Delay	t_{SCF}		—	—	40	40	ns
XFR Active Delay	t_{XFR}		—	—	50	50	ns
XFR Inactive Delay	t_{XFF}		—	—	50	50	ns
ZO Delay Time	t_{ZD}		—	—	50	50	ns
I Delay Time	t_{ID}		—	—	50	50	ns
MA Delay Time	t_{MAD}		—	—	50	50	ns
ZI Setup Time	t_{ZIS}		25	25	—	—	ns
ZI Hold Time	t_{ZIH}		0	0	—	—	ns
M/$\overline{I}$ Active Delay	t_{SMF}		—	—	45	45	ns
M/$\overline{I}$ Inactive Delay	t_{SMR}		—	—	45	45	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}		$t_{CYCL} - 20$	$t_{CYCL} - 20$	$t_{CYCL} + 20$	$t_{CYCL} + 20$	ns

2378 Pgm tbl 27c

Read Modify Write

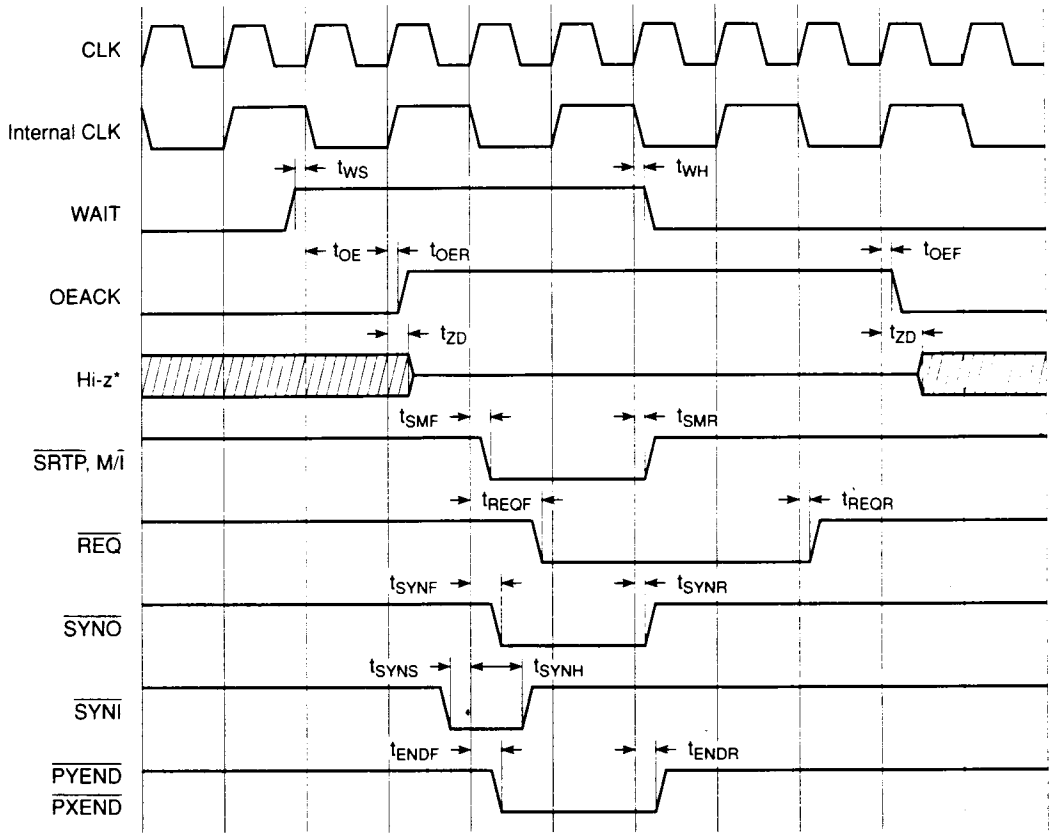


2378 Fhd 27f

PARAMETER	SYMBOL	CONDITION	MIN.		MAX.		UNIT
			12 MHz	16 MHz	12 MHz	16 MHz	
$\overline{REQ}$ Active Delay	t_{REQF}		—	—	60	55	ns
$\overline{REQ}$ Inactive Delay	t_{REQR}		—	—	60	55	ns
$\overline{DTOEI}$, $\overline{DTOEZ}$ Active Delay (from CLK down edge)	t_{DTF}		—	—	50	40	ns
$\overline{DTOEI}$, $\overline{DTOEZ}$ Inactive Delay (from CLK down edge)	t_{DTR}		—	—	50	40	ns
RD/$\overline{WD}$ Active Delay	t_{RDF}		—	—	40	40	ns
RD/$\overline{WD}$ Inactive Delay	t_{RDR}		—	—	40	40	ns

2378 Pgm tbl 27e

Wait Timing and Synchronous Timing



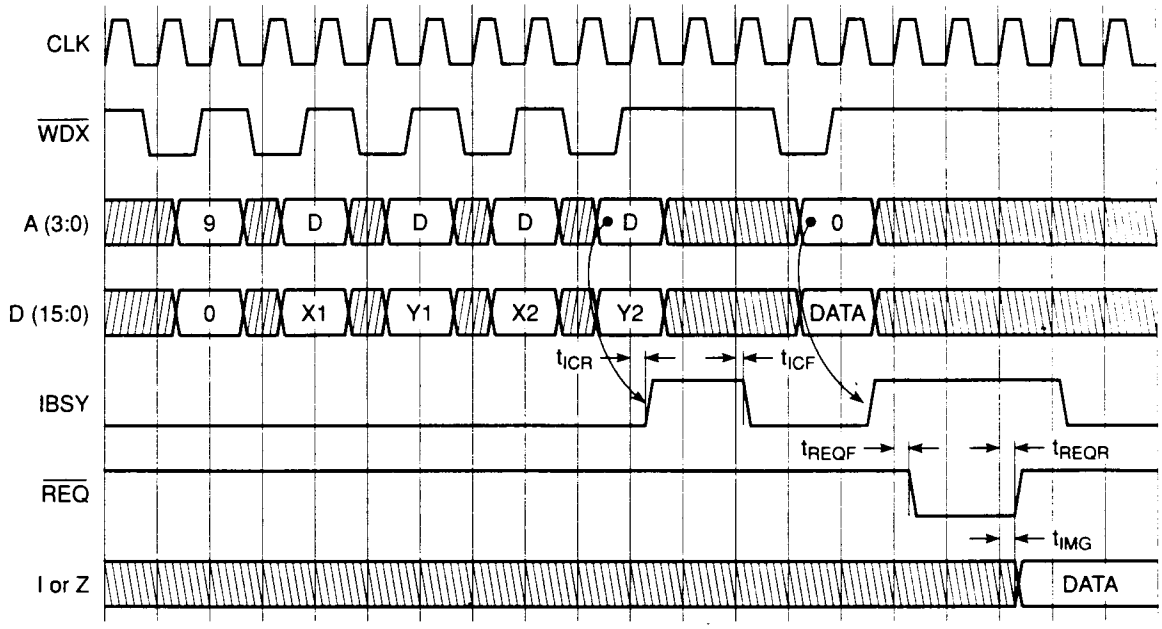
Hi-z pin: MA (25:0), I (15:0), Z0 (15:0), $\overline{RAS}$, $\overline{CAS}$, $\overline{DTOE}$, $\overline{WEZS}$, $\overline{WEZ}$, $\overline{WEI}$

2378 Fhd 27h

PARAMETER	SYMBOL	CONDITION	MIN.		MAX.		UNIT
			12 MHz	16 MHz	12 MHz	16 MHz	
WAIT Setup Time	t_{WS}		5	5	—	—	ns
WAIT Hold Time	t_{WH}		20	20	—	—	ns
WAIT to OEACK Delay Time	t_{OE}		—	—	$13t_{CYC}$	$13t_{CYC}$	ns
OEACK Active Delay	t_{OER}		—	—	45	45	ns
OEACK Inactive Delay	t_{OEF}		—	—	40	40	ns
PIN Float/Valid Delay	t_{ZD}		—	—	60	50	ns
$\overline{SRTP}$, M/I Active Delay	t_{SMF}		—	—	50	50	ns
$\overline{SRTP}$, M/I Inactive Delay	t_{SMR}		—	—	50	50	ns
$\overline{SYNO}$ Active Delay	t_{SYNF}		—	—	40	40	ns
$\overline{SYNO}$ Inactive Delay	t_{SYNR}		—	—	40	40	ns
$\overline{SYNI}$ Set-up Time	t_{SYNS}		30	30	—	—	ns
$\overline{SYNI}$ Hold Time	t_{SYNH}		30	30	—	—	ns
PY, PXEND Inactive Delay	t_{ENDF}		—	—	50	50	ns
PY, PXEND Active Delay	t_{ENDR}		—	—	50	50	ns

2378 Pgm tbl 27g

Image Data Input and Output

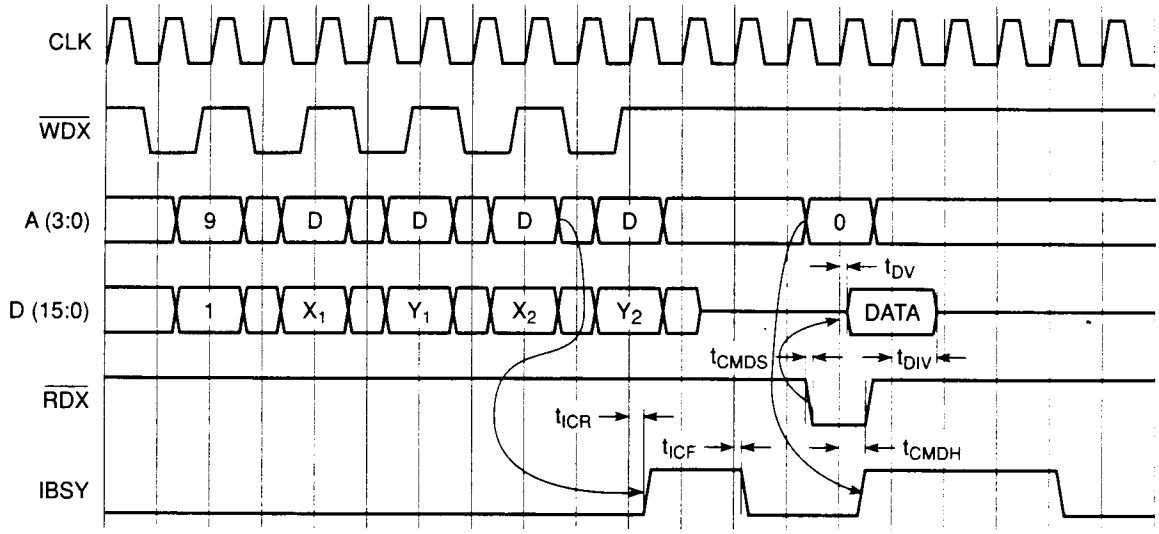


2378 Fhd 27m

Image Data Output

PARAMETER	SYMBOL		CONDITION	MIN.		MAX.		UNIT
				12 MHz	16 MHz	12 MHz	16 MHz	
IBSY Active Delay	t_{ICR}	t_{ICR}		—	—	50	50	ns
IBSY Inactive Delay	t_{ICF}	t_{ICF}		—	—	50	50	ns
Data Valid Delay	t_{DV}	t_{RDE}		—	—	40	30	ns
Data Invalid Delay	t_{DIV}	t_{RDH}		—	10	60	—	ns
Z.I. Delay	t_{IMG}	t_{IMG}		—	—	40	40	ns

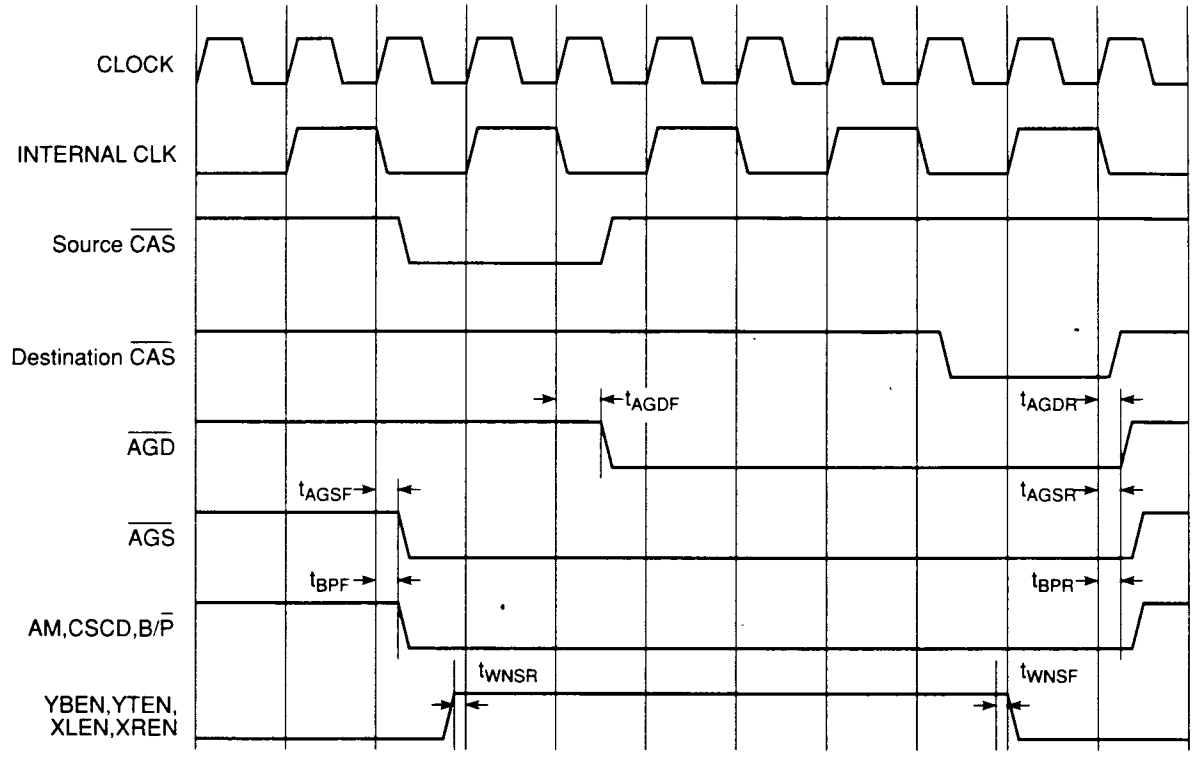
2378 Pgm tbl 27



2378 Fhd 27j

Image Data Input

Address Generator



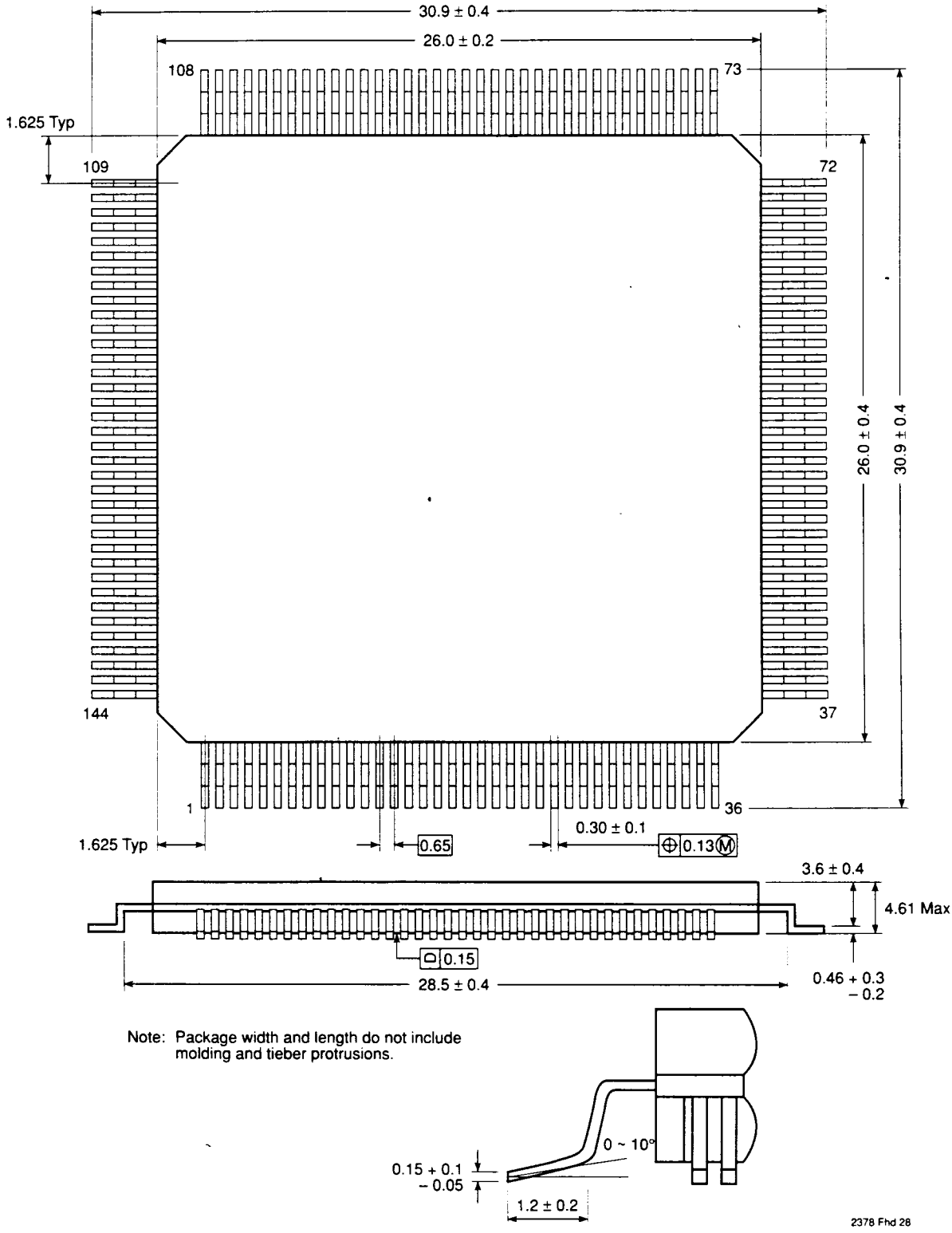
2378 Fhd 27l

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
$\overline{AGD}$ Active Delay	t_{AGDF}		—	50	ns
$\overline{AGD}$ Inactive Delay	t_{AGDR}		—	50	ns
$\overline{AGS}$ Active Delay	t_{AGSF}		—	50	ns
$\overline{AGS}$ Inactive Delay	t_{AGSR}		—	50	ns
AM, B/P Rise Time	t_{BPF}		—	50	ns
AM, B/P Fall Time	t_{BPF}		—	50	ns
YBEN, YTEN, XLEN, M XREN Inactive Delay	t_{WNSR}		—	50	ns
YBEN, YTEN, XLEN, M XREN Active Delay	t_{WNSF}		—	50	ns

2378 Pgm tbl 27k

Package Dimensions

QPF144-G-2626 Unit: mm



Note: Package width and length do not include molding and tieber protrusions.

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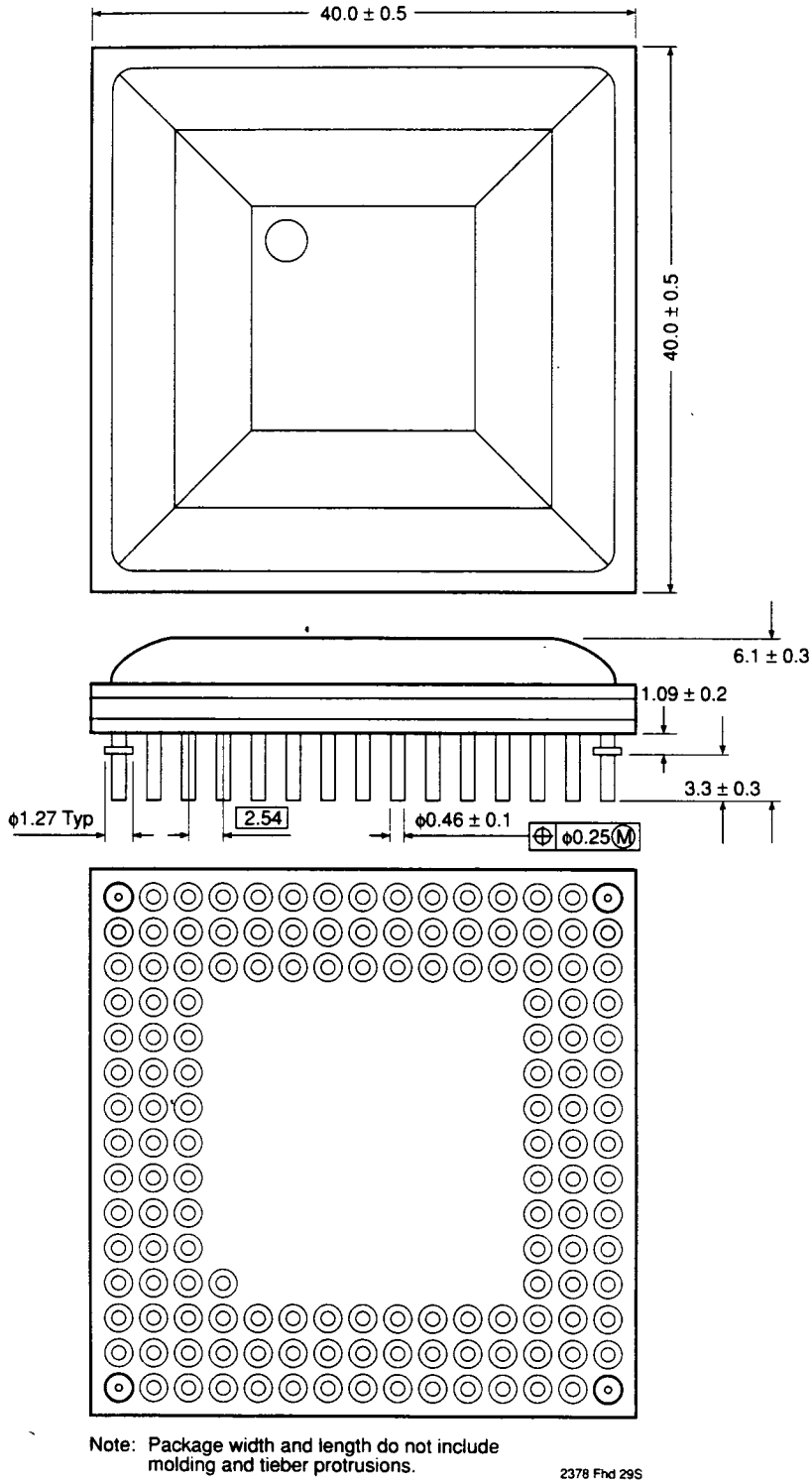
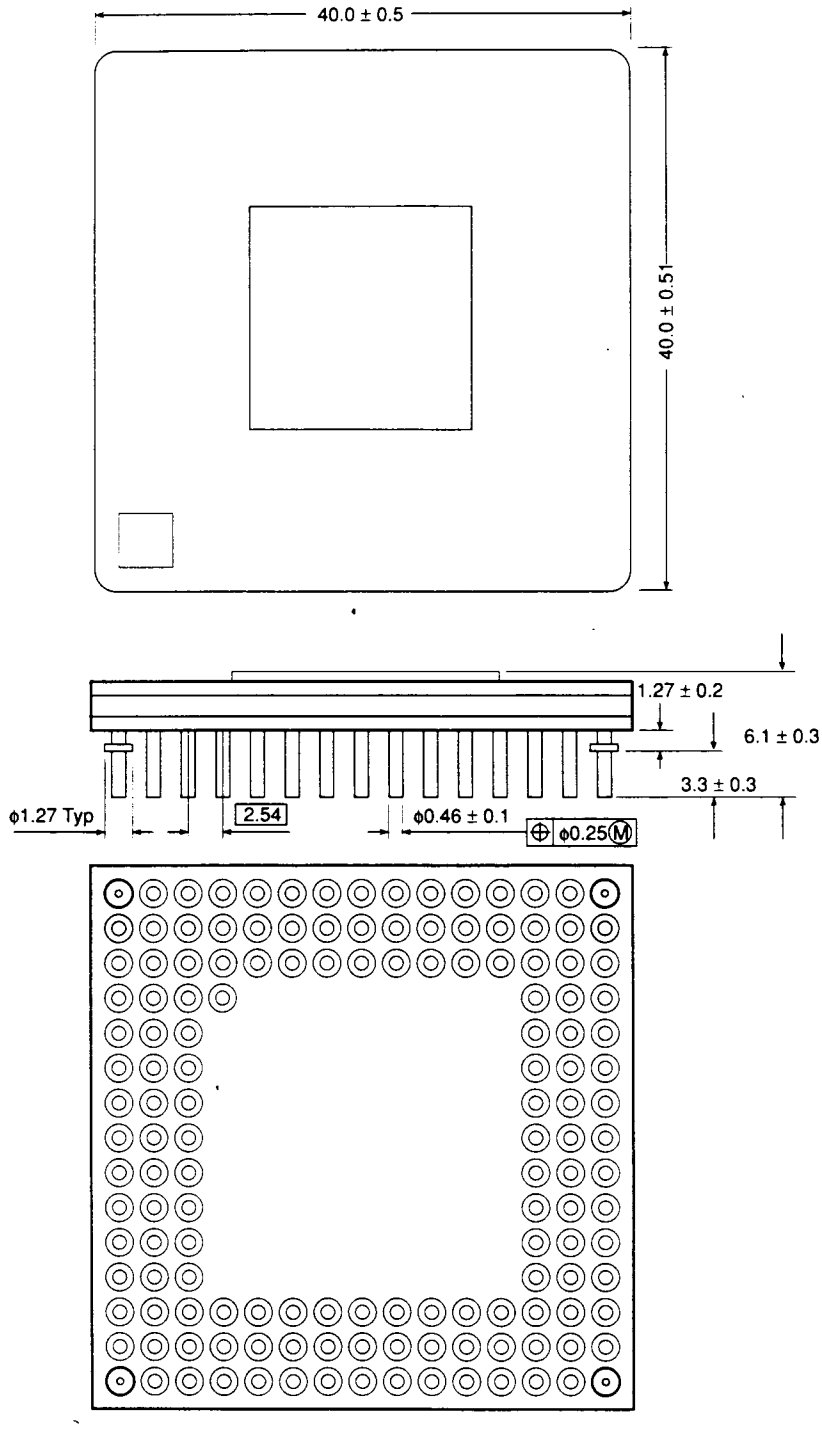
PGA144-M-S15U Unit: mm



Note: Package width and length do not include molding and tieber protrusions.

2378 Fhd 29S

PGA144-C-S15U Unit: mm



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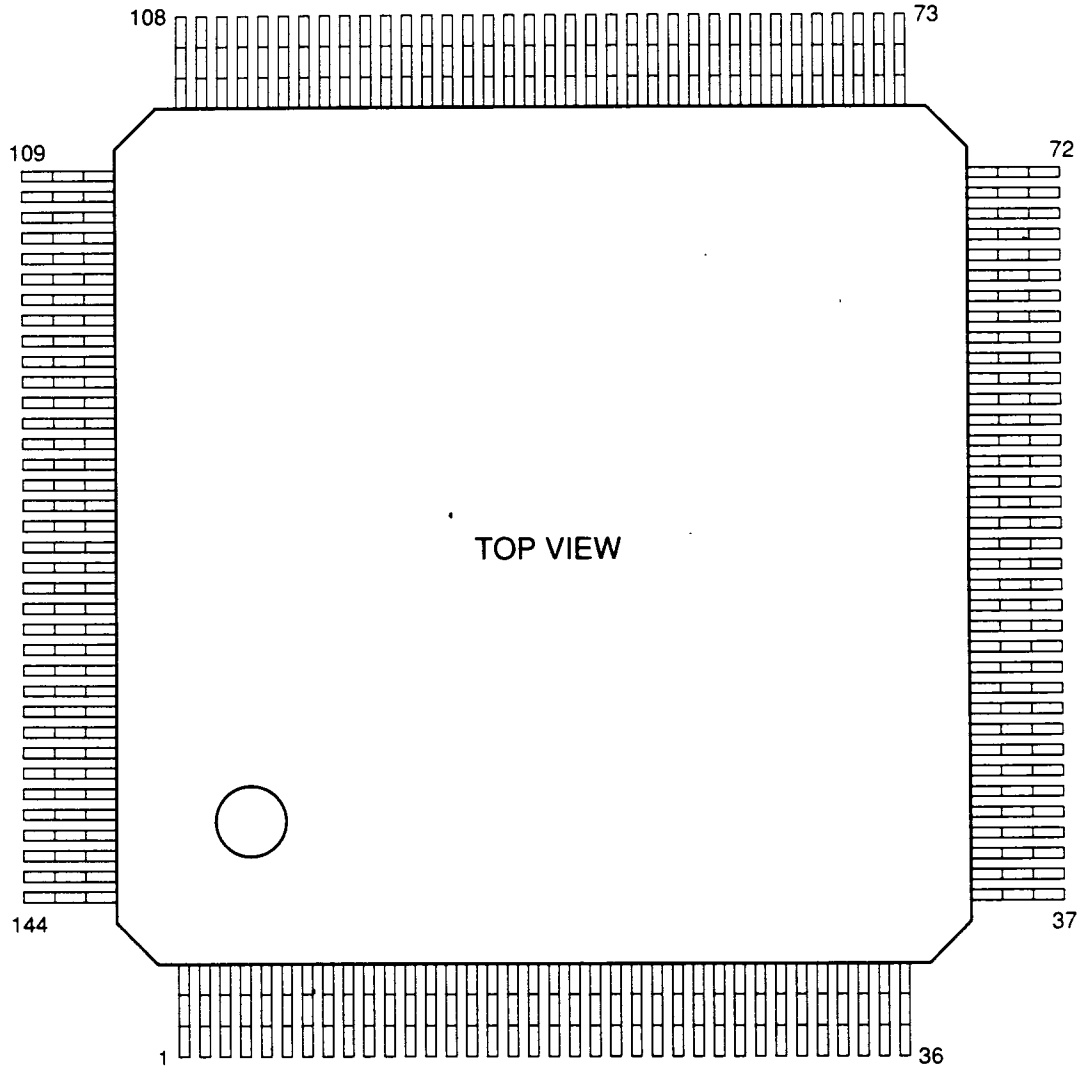
Pin Locations

144-Pin Ceramic Quad Flat Package



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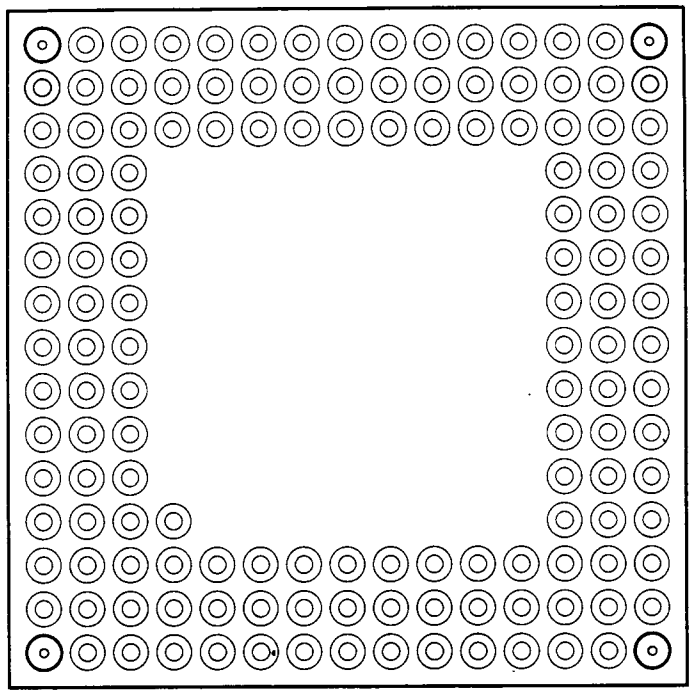
144-Pin Metal/Ceramic PGA Package



2378 Fhd 29S

15	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29
14	44	93	92	91	90	89	88	87	86	85	84	83	82	81	28
13	45	94	135	134	133	132	131	130	129	128	127	126	125	80	27
12	46	95	136										124	79	26
11	47	96	137										123	78	25
10	48	97	138										122	77	24
9	49	98	139										121	76	23
8	50	99	140				TOP VIEW						120	75	22
7	51	100	141										119	74	21
6	52	101	142				EXTRA PIN						118	73	20
5	53	102	143										117	72	19
4	54	103	144										116	71	18
3	55	104	105	106	107	108	109	110	111	112	113	114	115	70	17
2	56	57	58	59	60	61	62	63	64	65	66	67	68	69	16
1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

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Ordering Codes

TC8512G

- G – Ceramic Quad Flat-pack (QPF)
- YM – Metal Pin Grid Array (PGA)
- Y – Ceramic Pin Grid Array (PGA)

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