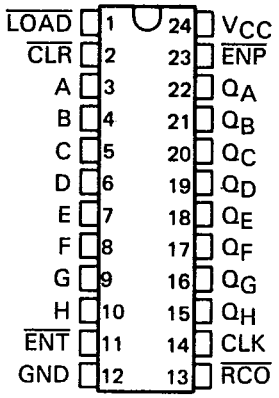
SN54ALS8161, SN74ALS8161
SYNCHRONOUS 8-BIT BINARY COUNTER

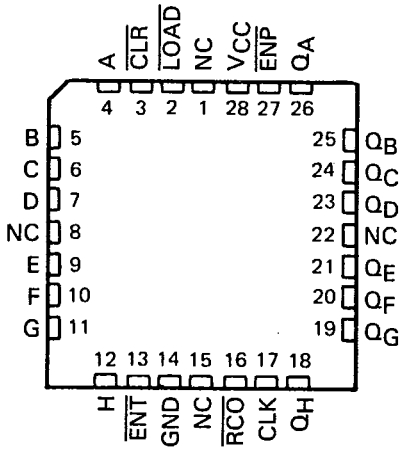
D2990, JANUARY 1987

- **Internal Look-Ahead for Fast Counting**
- **Carry Output for N-Bit Cascading**
- **Asynchronous Clearing**
- **Synchronous Counting or Loading**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS8161 . . . J PACKAGE
SN74ALS8161 . . . N PACKAGE
(TOP VIEW)



SN54ALS8161 . . . FK PACKAGE
SN74ALS8161 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

This synchronous, presettable counter features an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the eight flip-flops on the rising (positive-going) edge of the clock input waveform.

This counter is fully programmable; that is, it may be preset to any number between 0 and 255. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the level of the enable inputs.

The clear function is asynchronous, and a low level at the clear input sets all eight of the flip-flop outputs low, regardless of the level of the load or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs ($\overline{ENP}$ and $\overline{ENT}$) must be low to count, and $\overline{ENT}$ is fed forward to enable the ripple carry output. The ripple carry output ($\overline{RCO}$) thus enabled will produce a low-level output pulse while the count is maximum (255 with Q_A high). This low-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the $\overline{ENP}$ or $\overline{ENT}$ inputs are allowed regardless of the level of the clock input.

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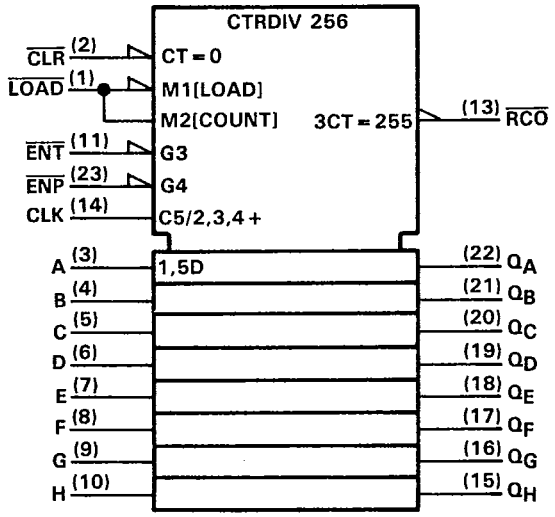
description (continued)

This counter features a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, or $\overline{LOAD}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, counting, or loading) will be dictated solely by the conditions meeting the stable setup and hold times.

The SN54ALS8161 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS8161 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbes are for J or N packages.

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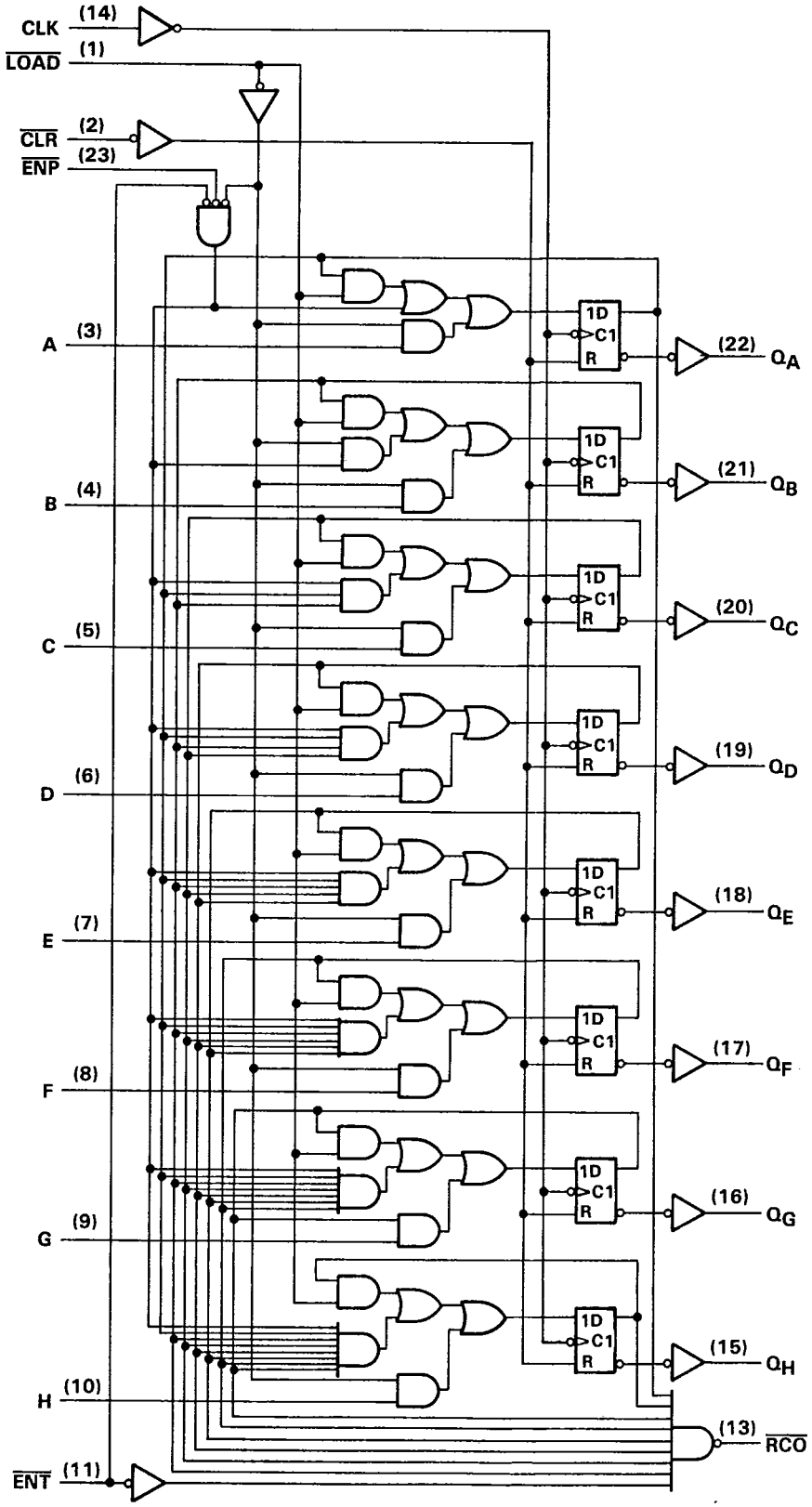
logic diagram (positive logic)

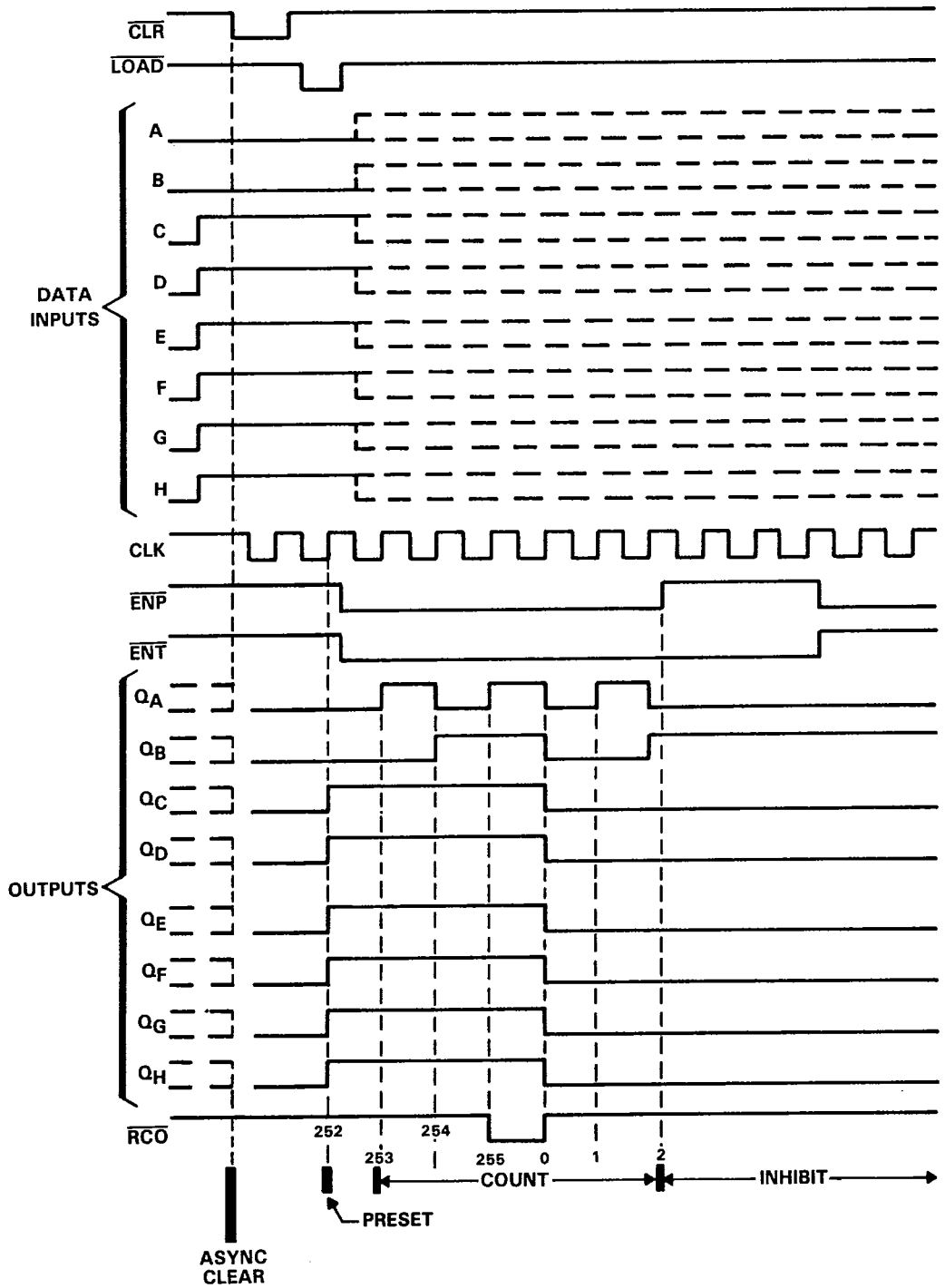


Pin numbers shown are for J or N packages.

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to binary 252
3. Count to 253, 254, 255, 0, 1, and 2
4. Inhibit (first with $\overline{ENP}$, then with $\overline{ENT}$)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS8161 . . . . . −55°C to 125°C
SN74ALS8161 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS8161			SN74ALS8161			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		30	0		35	MHz
t_w	Pulse duration	CLK high or low	16.5			14			ns
		$\overline{CLR}$ low	20			15			
t_{su}	Setup time before CLK↑	Data inputs A–H	15			10			ns
		$\overline{LOAD}$	15			10			
		$\overline{ENP}$, $\overline{ENT}$	17			15			
		$\overline{CLR}$ high (inactive)	10			10			
t_h	Hold time, all synchronous inputs after CLK↑		0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS8161			SN74ALS8161			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			25	40		25	40	mA

† All typical numbers are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short circuit output current, I_{OS}.

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switching characteristics (see Note)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS8161			SN54ALS8161		SN74ALS8161		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}				40		30		35		MHz
t_{PLH}	CLK	$\overline{RCO}$		7	10	3	15	3	13	ns
t_{PHL}				7	10	3	15	3	13	
t_{PLH}	CLK	Any Q		7	10	3	18	3	15	ns
t_{PHL}				10	14	4	20	4	17	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$		7	10	3	15	3	13	ns
t_{PHL}				4	7	1	10	1	9	
t_{PHL}	$\overline{CLR}$	Any Q		11	15	6	22	6	19	ns
t_{PHL}	$\overline{CLR}$	$\overline{RCO}$		8	11	5	25	5	20	ns

NOTE: For load circuit and voltage waveforms, see Section 1 of *ALS/AS Logic Data Book*, 1986.