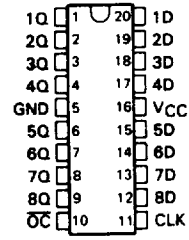
METASTABLE-RESISTANT OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D3060, FEBRUARY 1989

- **Meta-Flops™ Series — Metastable-Resistant Flip-Flops**
- **Specifically Designed for Data Synchronization Applications**
- **Improved Metastable Characteristics Provide Greater System Reliability**
- **3-State Outputs Drive Bus Lines Directly**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

The 'AS3374, a member of the Meta-Flops™ Series, is an 8-bit metastable-resistant bus interface circuit designed specifically for data synchronization applications where the normal setup and hold time specifications will frequently be violated.

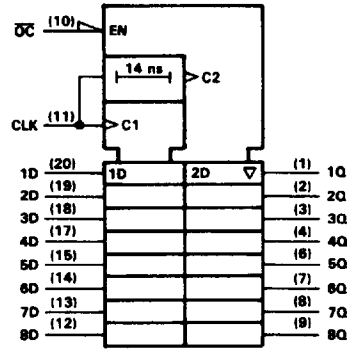
Synchronization of two digital signals operating at different frequencies is a common system dilemma. This problem is typically solved by synchronizing one of the signals to the local clock through a flip-flop. This solution, however, presents a problem. The setup and hold time specifications associated with the flip-flop's output are certain to be violated. Whenever the setup or hold times of a flip-flop are violated, its output response is uncertain. A flip-flop is metastable if its output hangs up in the region between V_{IL} and V_{IH}. The metastable state lasts until the flip-flop recovers into one of its two stable states. For conventional flip-flops, this recovery time can be longer than the specified propagation delay time.

Evaluating the metastable characteristics for a particular flip-flop is not an easy task. The number of times the output hangs up in the metastable region is extremely small compared to the total number of clock transitions.

Conventional test equipment is not designed to measure these parameters. Measuring these parameters on a production basis is impractical. Resistance to metastable failure is ensured by design only. For additional information on metastability, please refer to the application note located on page 4-51 of the *ALS/AS Logic Data Book*, 1986.

The SN74AS3374 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(EACH DUAL-RANK FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
H	X	X	Z
L	↑	L	L
L	↑	H	H
L	L	X	Q_0

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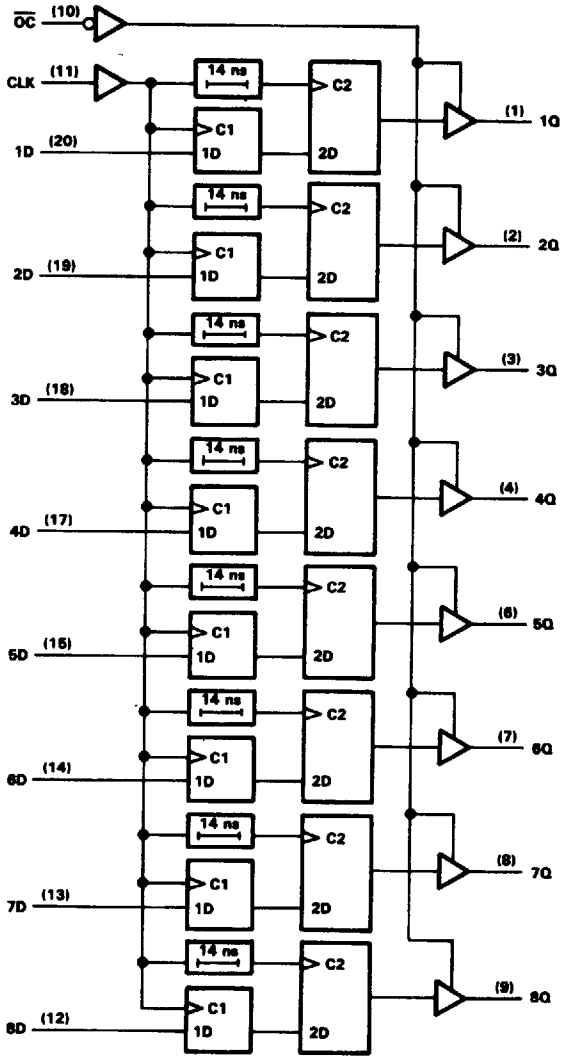
TEXAS INSTRUMENTS

logic diagram (positive logic)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current				48	mA
f_{clock}	Clock frequency		0		45	MHz
t_w	Pulse duration	CLK high	5			ns
		CLK low	5			
t_{su}	Setup time, data before CLK↑†		4			ns
t_h	Hold time, data after CLK↑†		2			ns
T_A	Operating free-air temperature		0		70	°C

† The data setup and hold times are specified for synchronous operation. These parameters also help guarantee overall speed characteristics of the device. Since production testing for metastability is impractical, conformance to conventional switching characteristics verifies metastable-failure resistance.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −3 mA	2.4	3.2		V
	V_{CC} = 4.75 V,	I_{OH} = −15 mA	2			
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 32 mA		0.25	0.4	V
	V_{CC} = 4.75 V,	I_{OL} = 48 mA		0.35	0.5	
I_I	V_{CC} = 5.25 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.4 V			−0.2	mA
I_{OZH}	V_{CC} = 5.25 V,	V_I = 2.4 V			20	μA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V			−20	μA
I_O§	V_{CC} = 5.25 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.25 V,	$\overline{OC}$ high		100	140	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 1)

PARAMETER	FROM	TO	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.75 V to 5.25 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}				50		45		MHz
t_{PLH}	CLK	Q		18	20	14	23	ns
t_{PHL}				18	20	14	23	
t_{PZH}	$\overline{OC}$	Q		7	9	2	11	ns
t_{PZL}				7	9	2	11	
t_{PHZ}	$\overline{OC}$	Q		5	7	1	8	ns
t_{PLZ}				5	7	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.