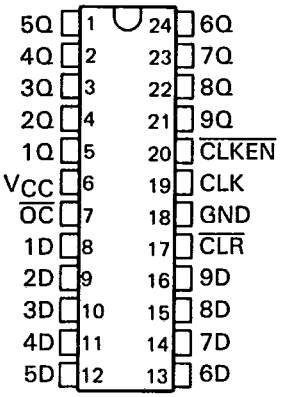
# SN74AS1823
# 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

APRIL 1987

- **Center $V_{CC}$ and GND Configuration Provides Minimum Lead Inductance in High Current Switching Applications**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Package Options Include Plastic DIPS. Use the 'AS823 for Plastic and Ceramic Chip Carriers and "Small Outline" Package Options**
- **Dependable Texas Instruments Quality and Reliability**

NT PACKAGE
(TOP VIEW)




FUNCTION TABLE

| INPUTS | | | | | OUTPUT |
|---|---|---|---|---|---|
| $\overline{OC}$ | $\overline{CLR}$ | $\overline{CLKEN}$ | CLK | D | Q |
| L | L | X | X | X | L |
| L | H | L | ↑ | H | H |
| L | H | L | ↑ | L | L |
| L | H | H | X | X | $Q_0$ |
| H | X | X | X | X | Z |

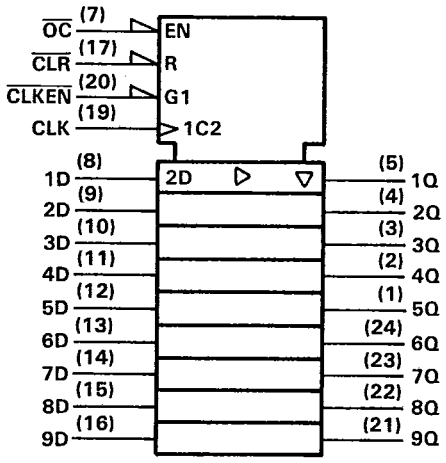
## description

This 9-bit flip-flop device features three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

With the clock enable ($\overline{CLKEN}$) low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The 'AS1823 has noninverting D inputs. Taking the $\overline{CLR}$ input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input ($\overline{OC}$)can be used to place the nine outputs in either normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

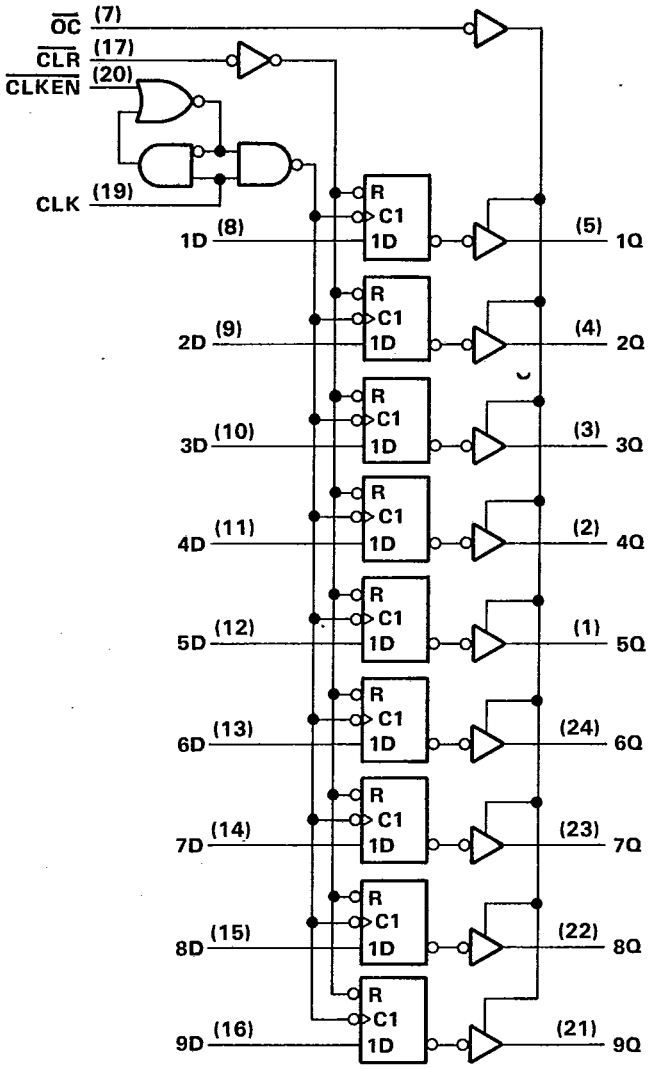
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

The SN74AS1823 is characterized for operation from 0°C to 70°C.

## logic diagram (positive logic)






TEXAS INSTRUMENTS
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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

### recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −24 | mA |
| $I_{OL}$ | Low-level output current | | | | 48 | mA |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 4 | | | ns |
| | | CLK high or low | 8 | | | |
| $t_{su}$ | Setup time before CLK↑ | $\overline{CLR}$ inactive | 8 | | | ns |
| | | Data | 6 | | | |
| | | $\overline{CLKEN}$ high or low | 6 | | | |
| $t_h$ | Hold time, $\overline{CLKEN}$ or data after CLK↑ | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −2 mA | $V_{CC}$−2 | | | V |
| | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −15 mA | 2.4 | 3.2 | | |
| | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −24 mA | 2 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 32 mA | | | | V |
| | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 48 mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | μA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | −50 | μA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.5 | mA |
| $I_O$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −30 | | −112 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V | Outputs high | | 49 | 80 | mA |
| | | Outputs low | | 61 | 100 | |
| | | Outputs disabled | | 64 | 103 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Note 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{PLH}$ | CLK | Any Q | 3.5 | 7.5 | ns |
| $t_{PHL}$ | | | 3.5 | 11 | |
| $t_{PHL}$ | $\overline{CLR}$ | Any Q | 3.5 | 13 | ns |
| $t_{PZH}$ | $\overline{OC}$ | Any Q | 4 | 11 | ns |
| $t_{PZL}$ | | | 4 | 12 | |
| $t_{PHZ}$ | $\overline{OC}$ | Any Q | 2 | 8 | ns |
| $t_{PLZ}$ | | | 2 | 8 | |

NOTE 1: Load circuit and voltage waveforms are shown in Section 1 of the *ALS/AS Logic Data Book, 1986.*