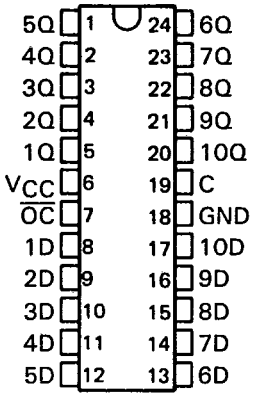
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

APRIL 1987

- **Center V_{CC} and GND Configuration Provides Minimum Lead Inductance in High Current Switching Applications**
- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus Structured Pinout**
- **Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity**
- **Buffered Control Inputs to Reduce DC Loading**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic DIPS. Use the 'AS841 for Plastic and Ceramic Chip Carriers and "Small Outline" Package Options.**
- **Dependable Texas Instruments Quality and Reliability**

NT PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

description

This 10-bit latch device features three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. It is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

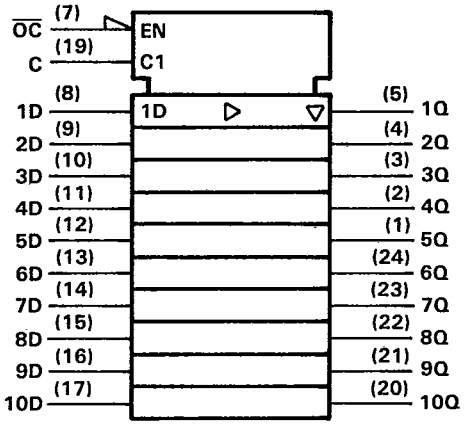
The ten latches are transparent D-type and have noninverting data (D) inputs.

A buffered output-control ($\overline{OC}$)input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

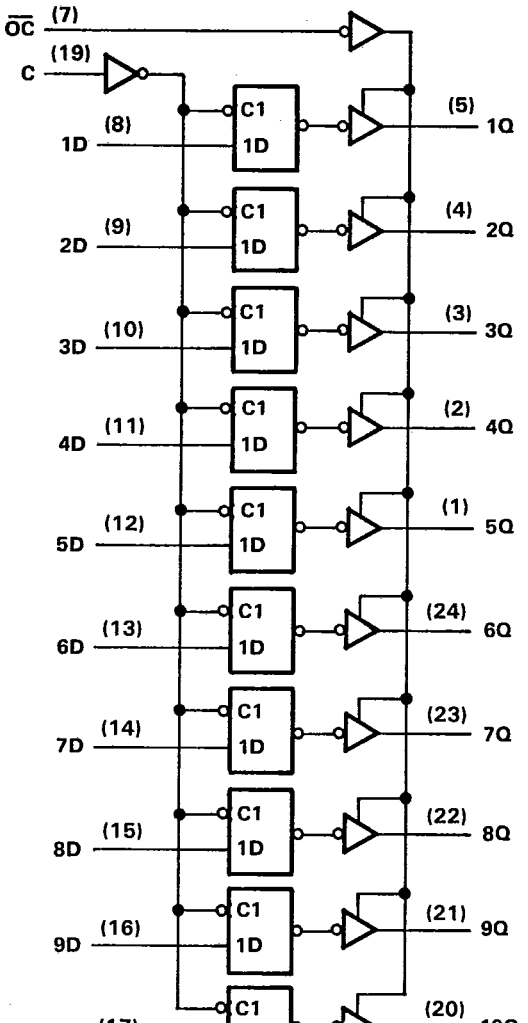
The SN74AS1841 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

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recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
t_w	Pulse duration, enable C high	4			ns
t_{su}	Setup time, data before enable C↓	2.5			ns
t_h	Hold time, data after enable C↓	2.5			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		36	60	mA
		Outputs low		58	94	
		Outputs disabled		56	92	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			MIN	MAX	
t_{PLH}	D	Q	1	6.5	ns
t_{PHL}			1	9	
t_{PLH}	C	Q	2	12	ns
t_{PHL}			2	12	
t_{PZH}	$\overline{OC}$	Q	2	10.5	ns
t_{PZL}			2	13.5	
t_{PHZ}	$\overline{OC}$	Q	1	8	ns
t_{PLZ}			1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1 of the *ALS/AS Logic Data Book, 1986.*